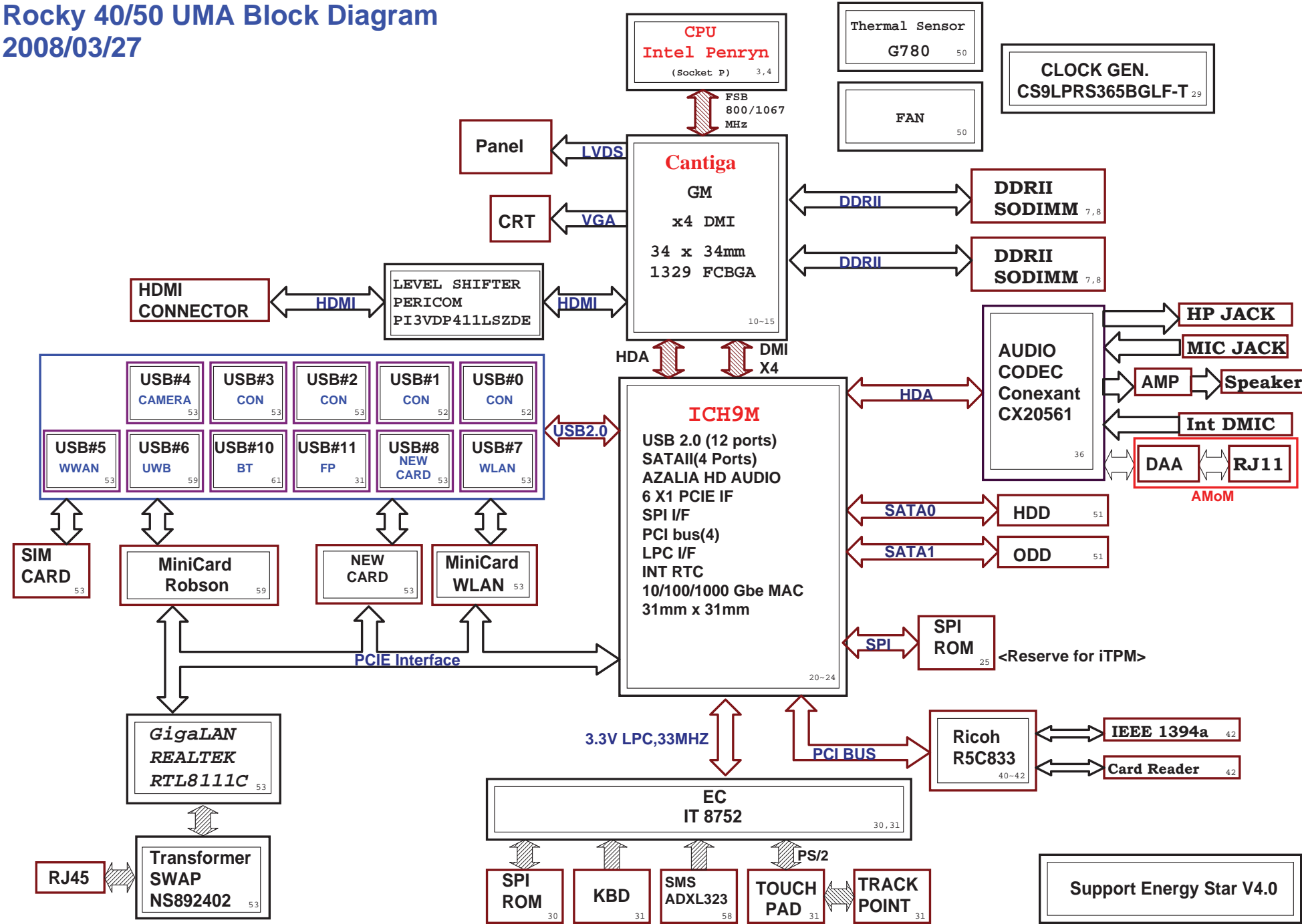
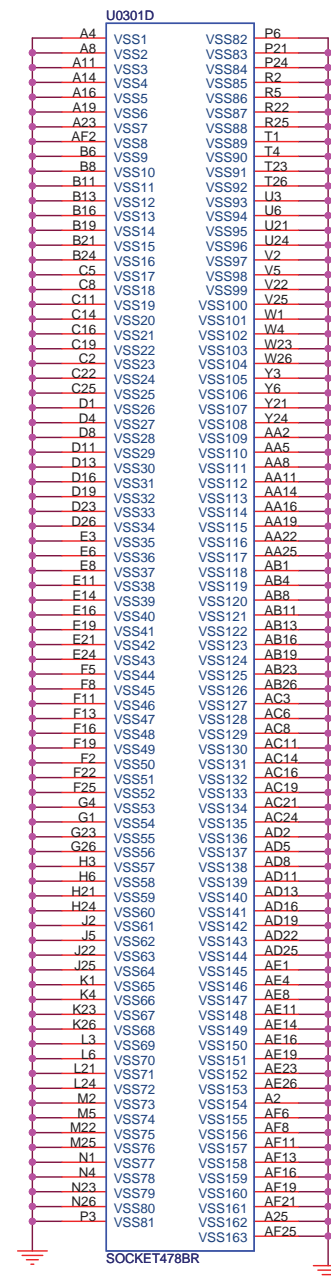


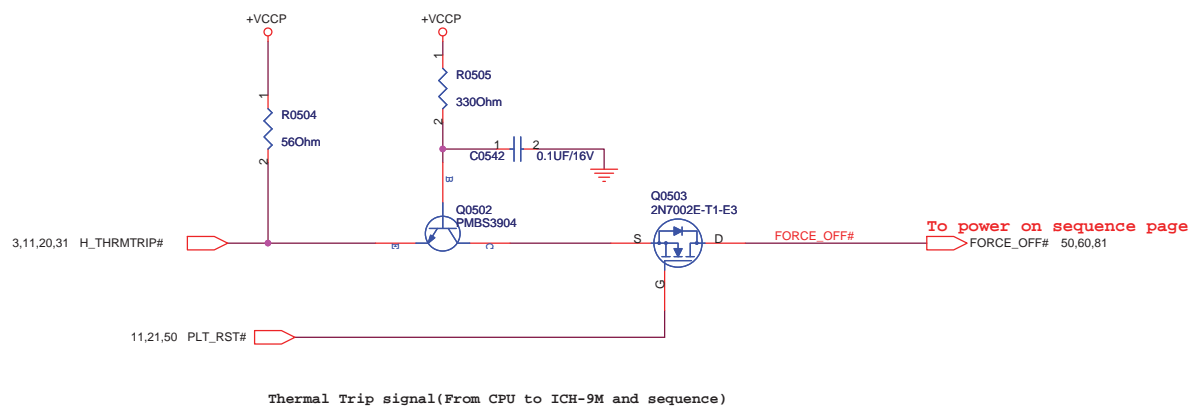
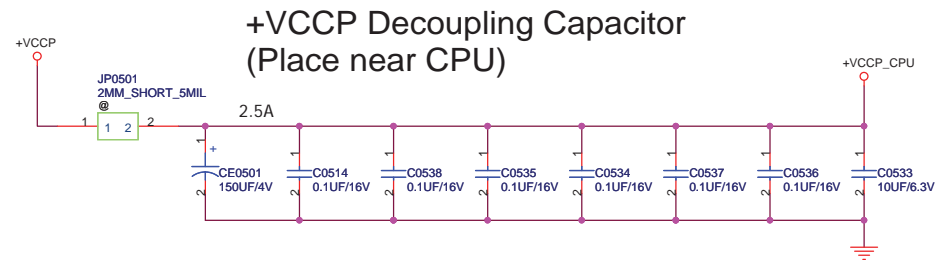
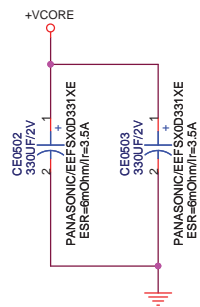
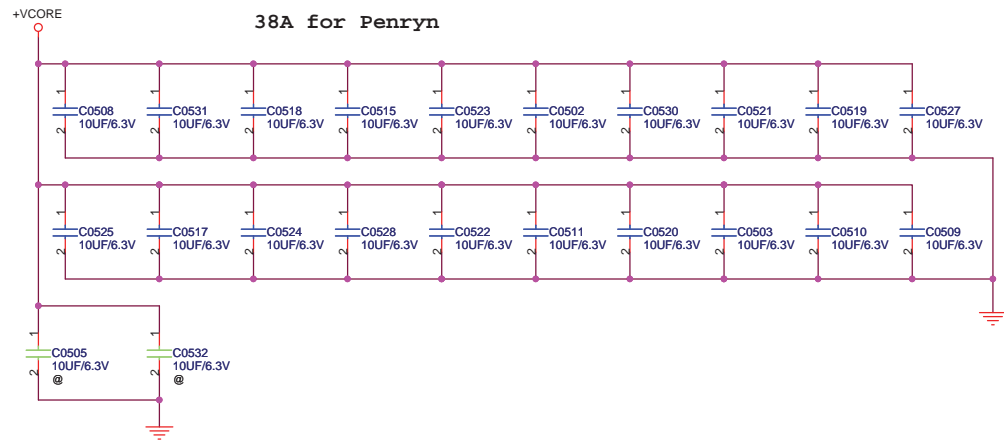
Rocky 40/50 UMA Block Diagram  
2008/03/27

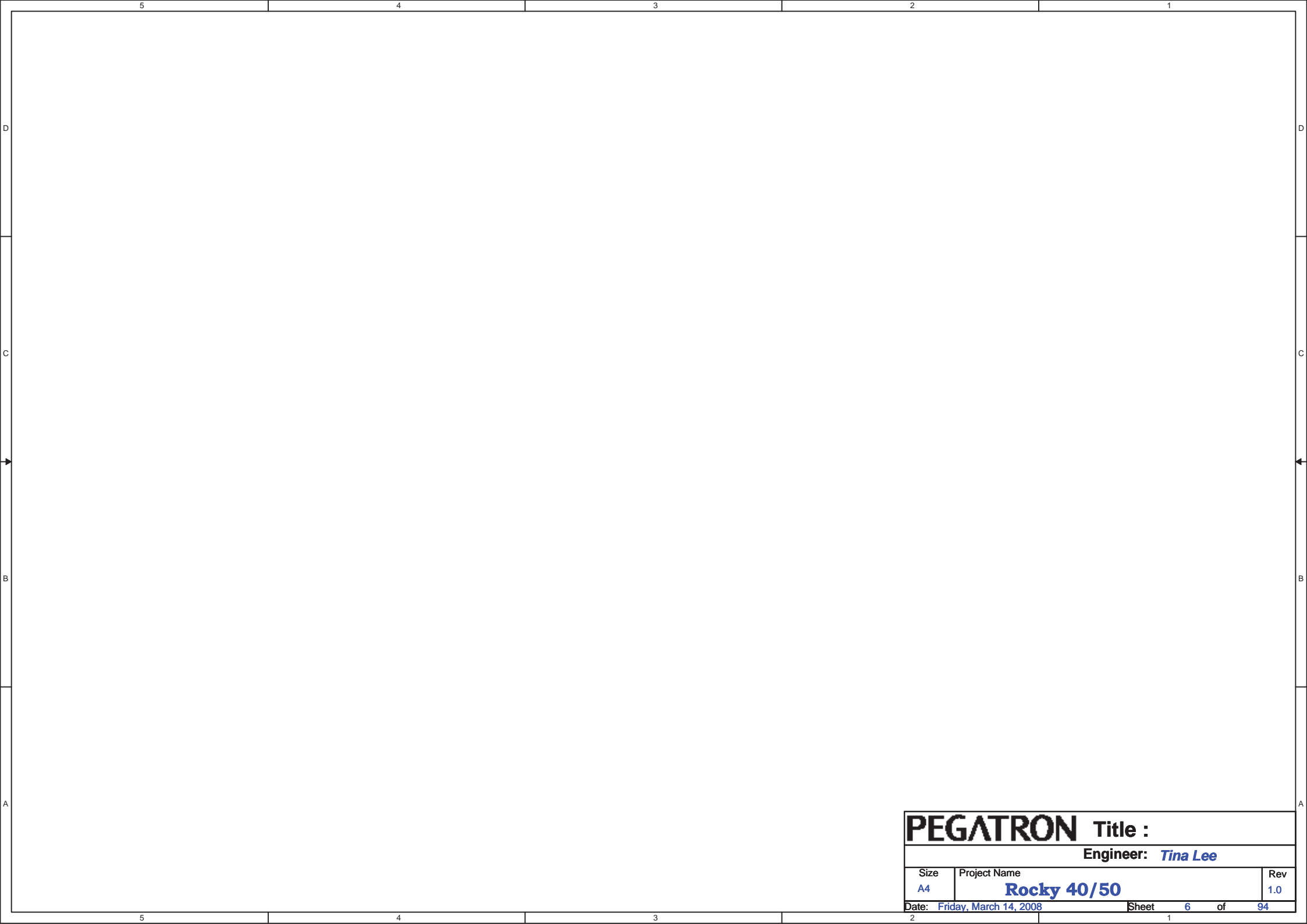












PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	6	of 94



SMBus Slave Address:A0H

temp\_5886\_t101  
(12G025M22000LV with 12G025C2200WLV  
co-lay symbol)

SMBus Slave Address: A0H

Place near SO-DIMM\_0

Layout Note: Place these caps near SO DIMM 0

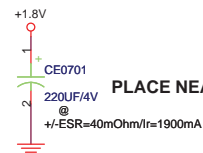
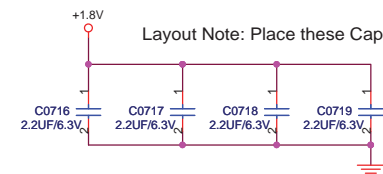
Layout Note: Place these Caps near SO DIMM 0

PLACE NEAR SO-DIMM\_0 / SO-DIMM\_1

Layout Note: Place these caps near SO DIMM 0

VREF -> 10/10 mils

SO-DIMM 0 is placed nearer the  
GMCH than SO-DIMM 1

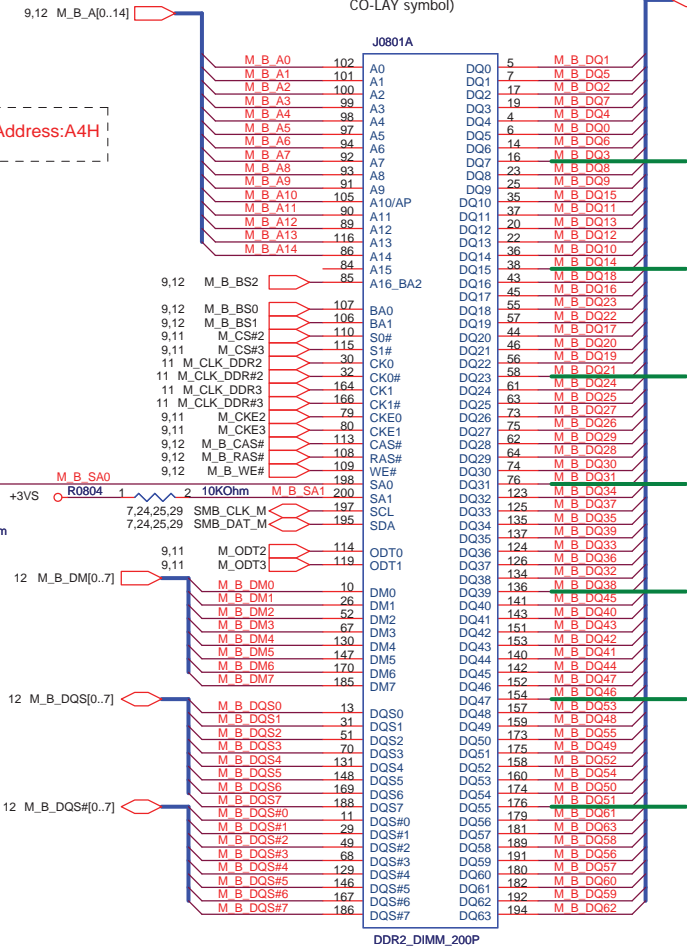
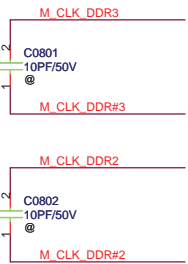




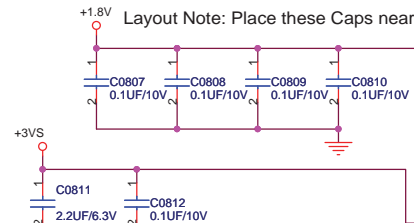
temp\_5886\_t102  
(12G025032005LV with 12G025022004LV  
CO-LAY symbol)

SMBus Slave Address:A4H

Place near SO-DIMM\_1

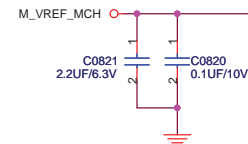


Layout Note: Place these Caps near SO DIMM 1

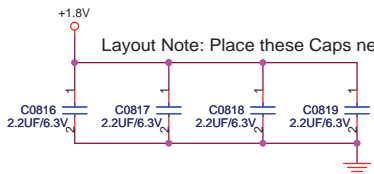






Layout Note: Place these Caps near SO DIMM 1

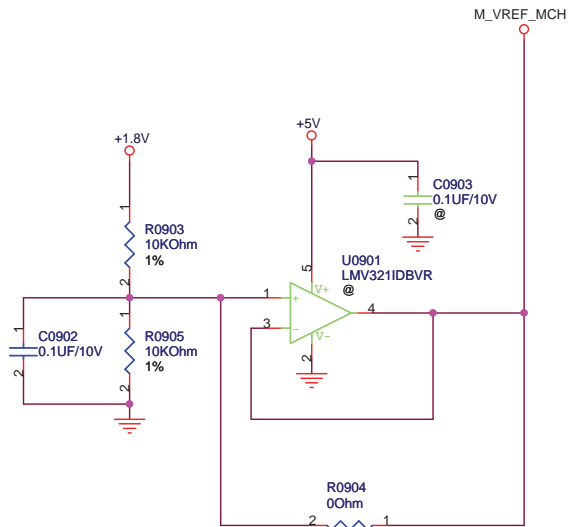
VREF -> 10/10 mils



Layout Note: Place these Caps near the SO-DIMM\_1



+5V  +5V 44,56,57,91  
 +1.8V  +1.8V 7,8,11,13,83,91  
 M\_VREF\_MCH  M\_VREF\_MCH 7,8,11  
 +0.9VS  +0.9VS 83



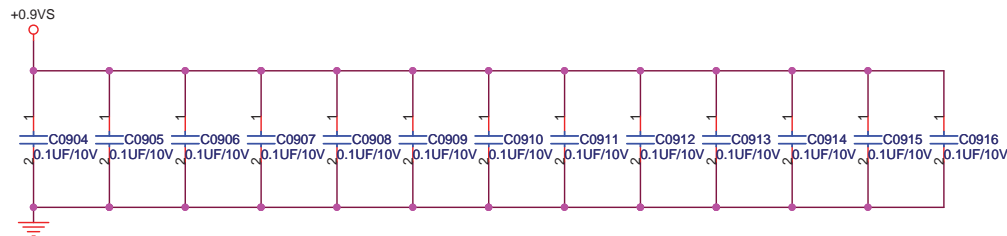
 M\_A\_A[0..13] 7,12  
 M\_A\_BS[0..2] 7,12

 M\_A\_CAS# 7,12  
 M\_A\_RAS# 7,12  
 M\_A\_WE# 7,12

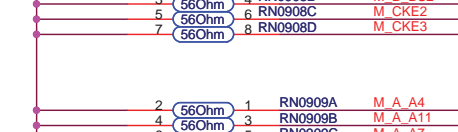
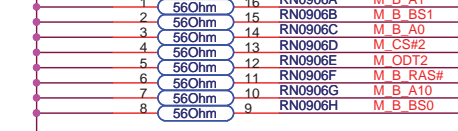
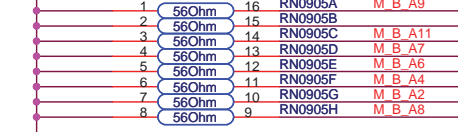
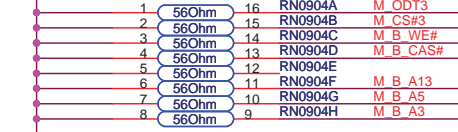
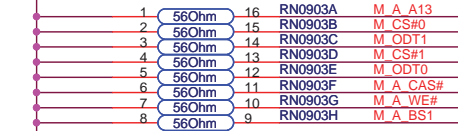
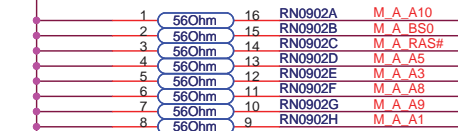
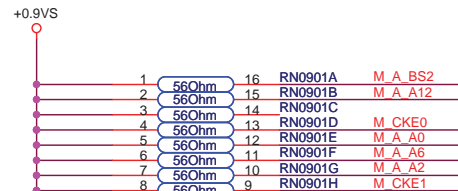
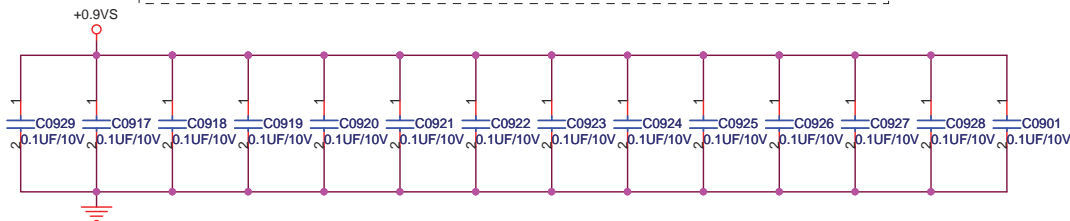
 M\_B\_A[0..13] 8,12  
 M\_B\_BS[0..2] 8,12

 M\_B\_CAS# 8,12  
 M\_B\_RAS# 8,12  
 M\_B\_WE# 8,12

 M\_CS#[0..3] 7,8,11  
 M\_ODT[0..3] 7,8,11  
 M\_CKE[0..3] 7,8,11



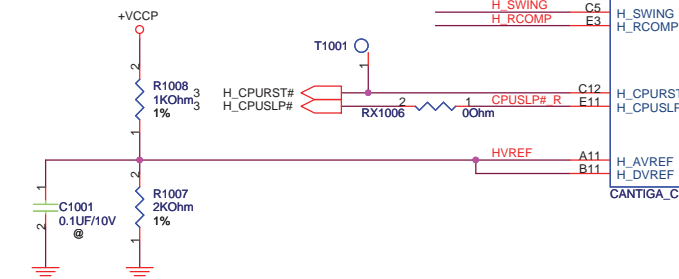
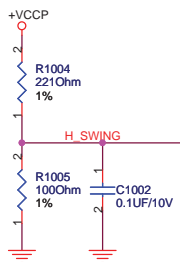
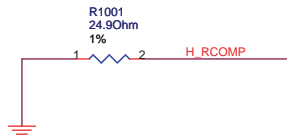
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



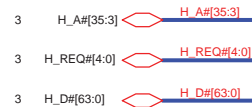
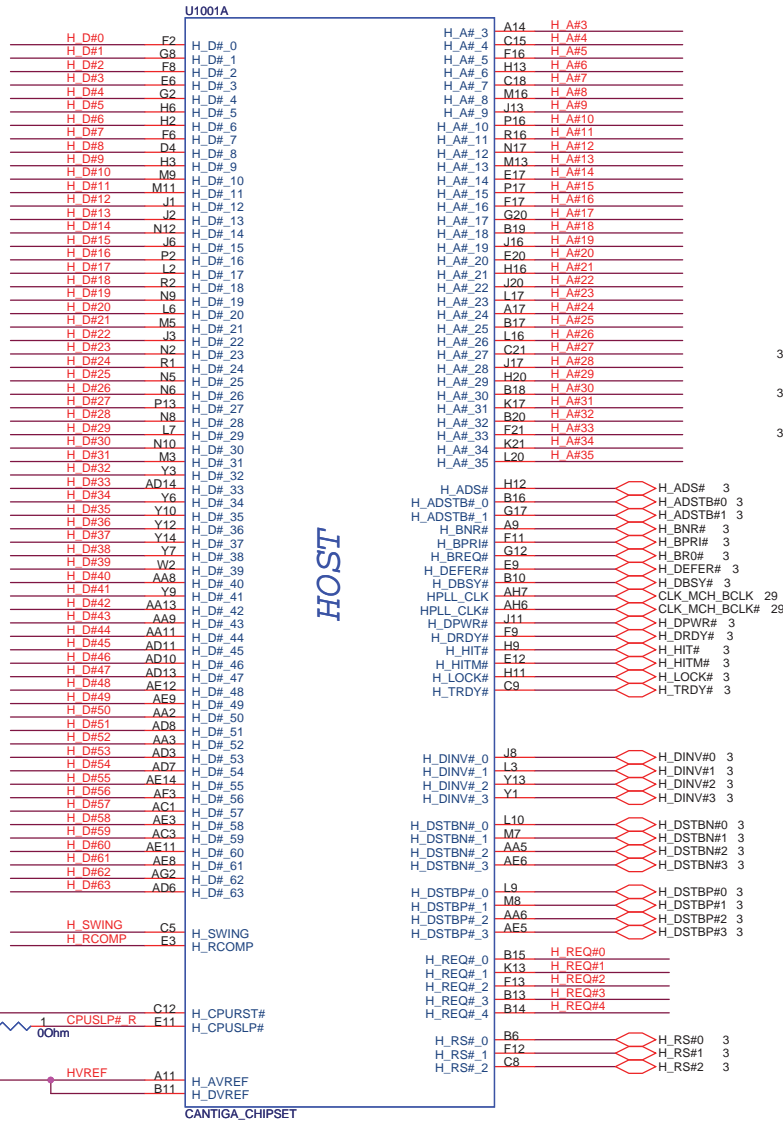
**PEGATRON** Title : **DDR2 VREF**

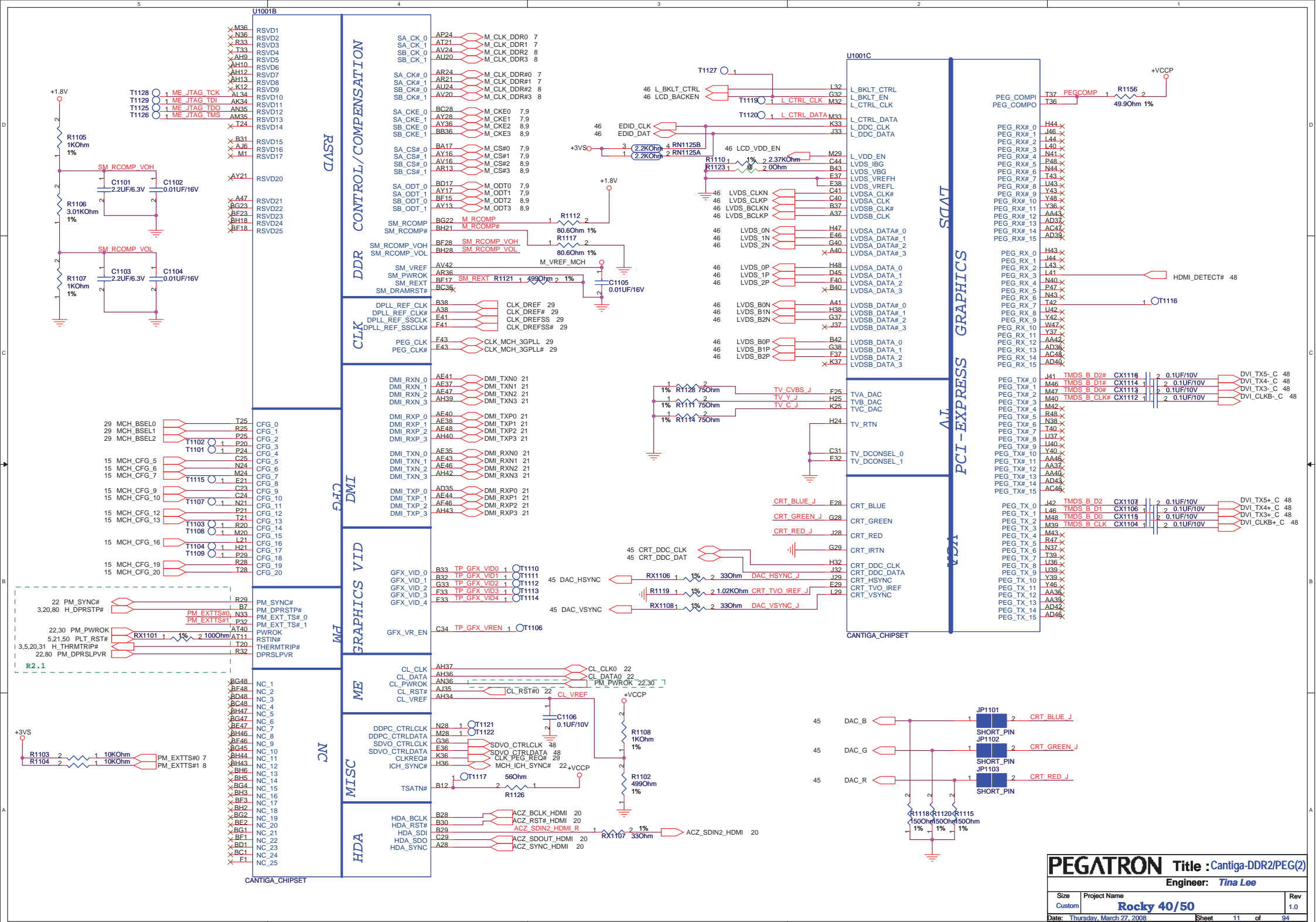
Engineer: **Tina Lee**

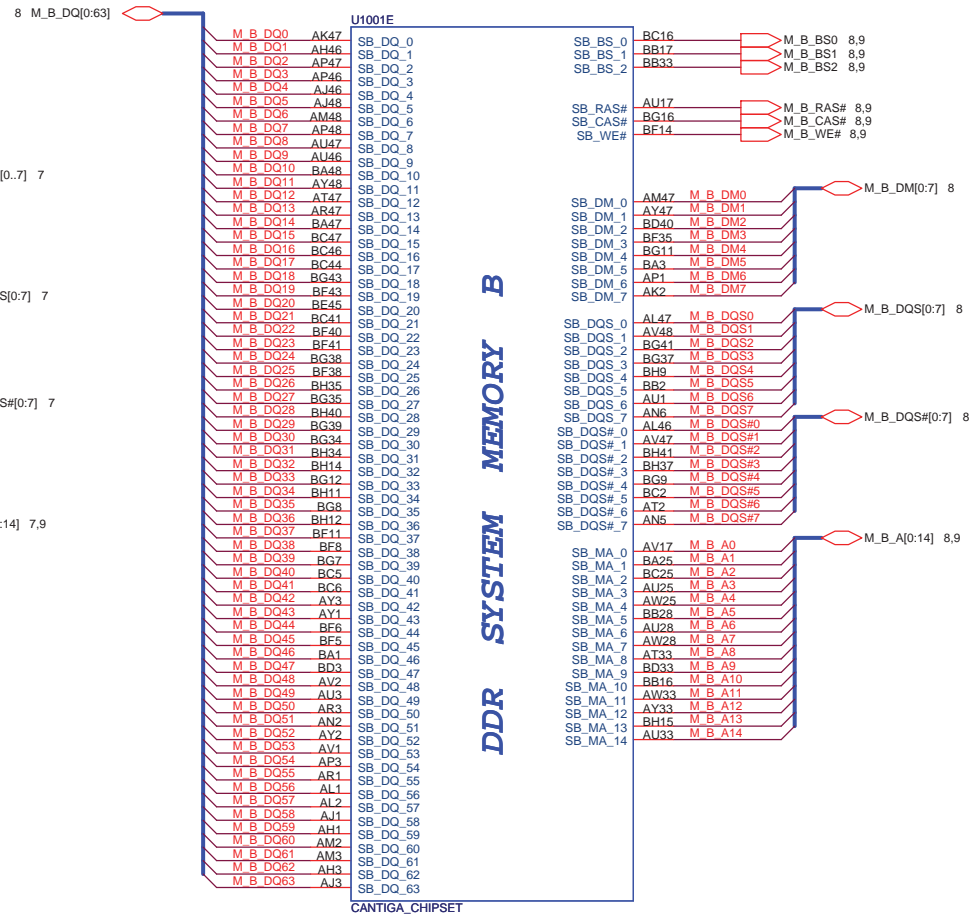
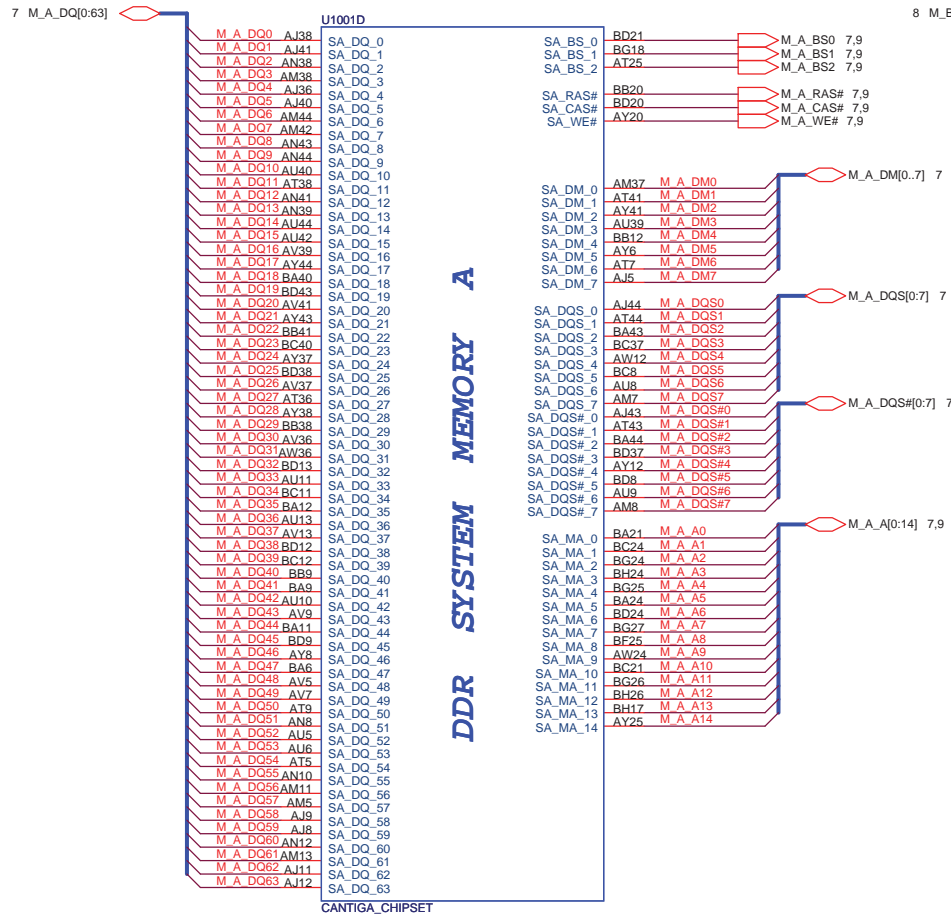
Size Custom	Project Name <b>Rocky 40/50</b>	Rev 1.0
Date: Thursday, March 27, 2008	Sheet 9 of 94	

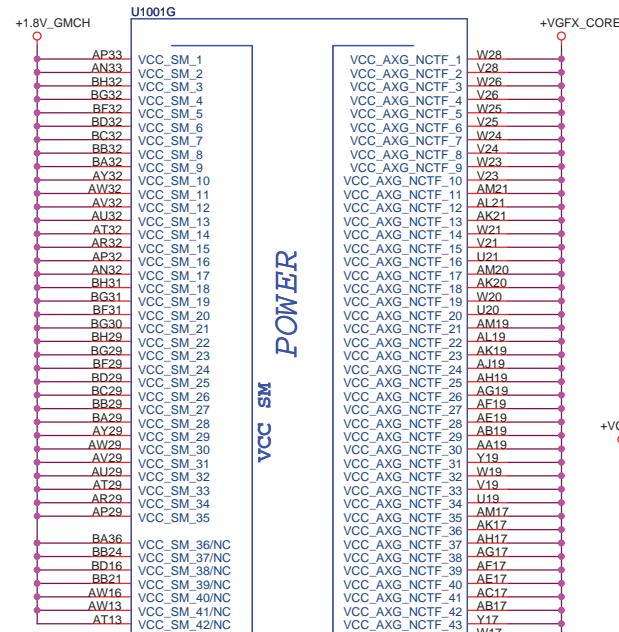


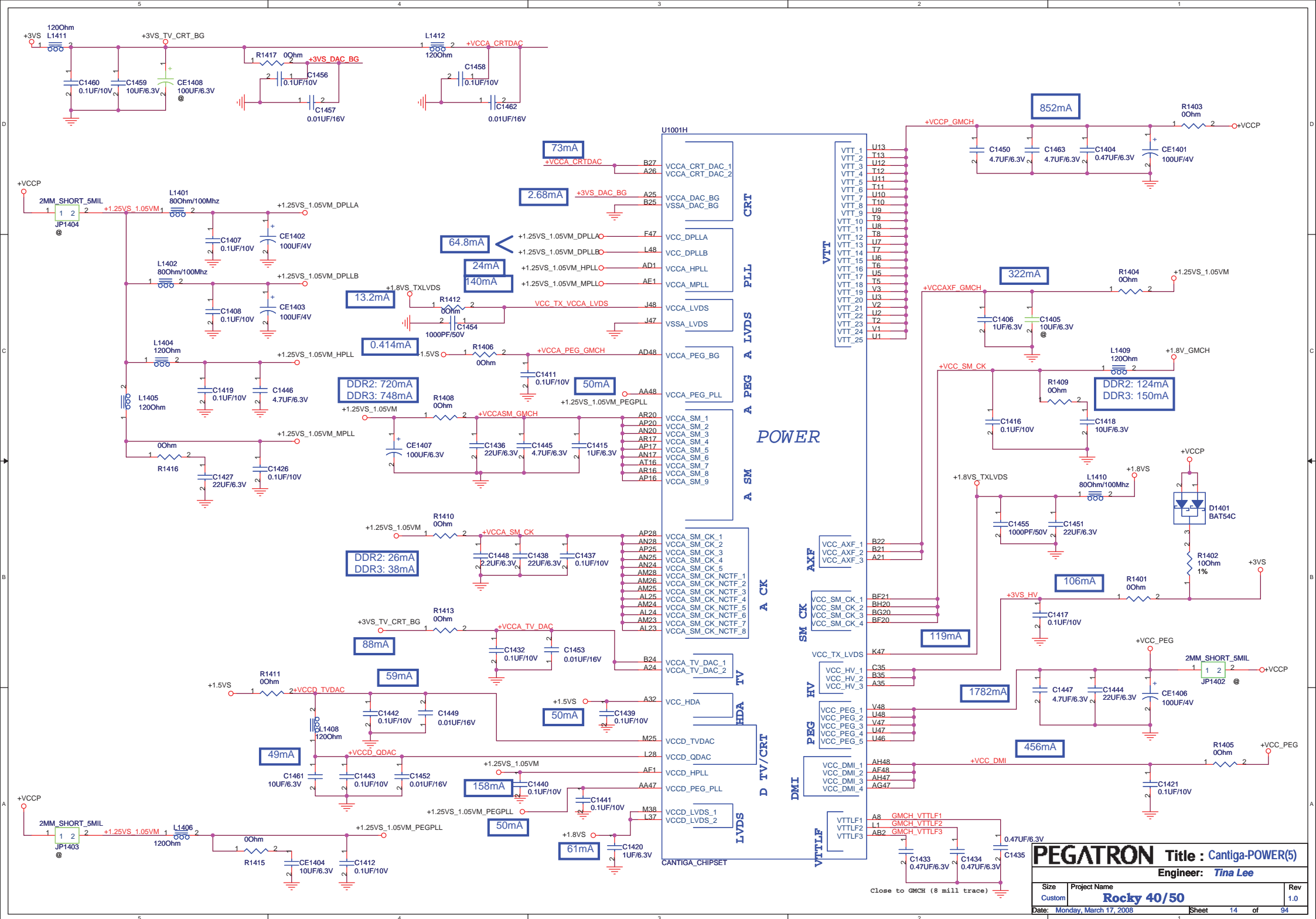
CAP 0.1U within 100 mils from GMCH

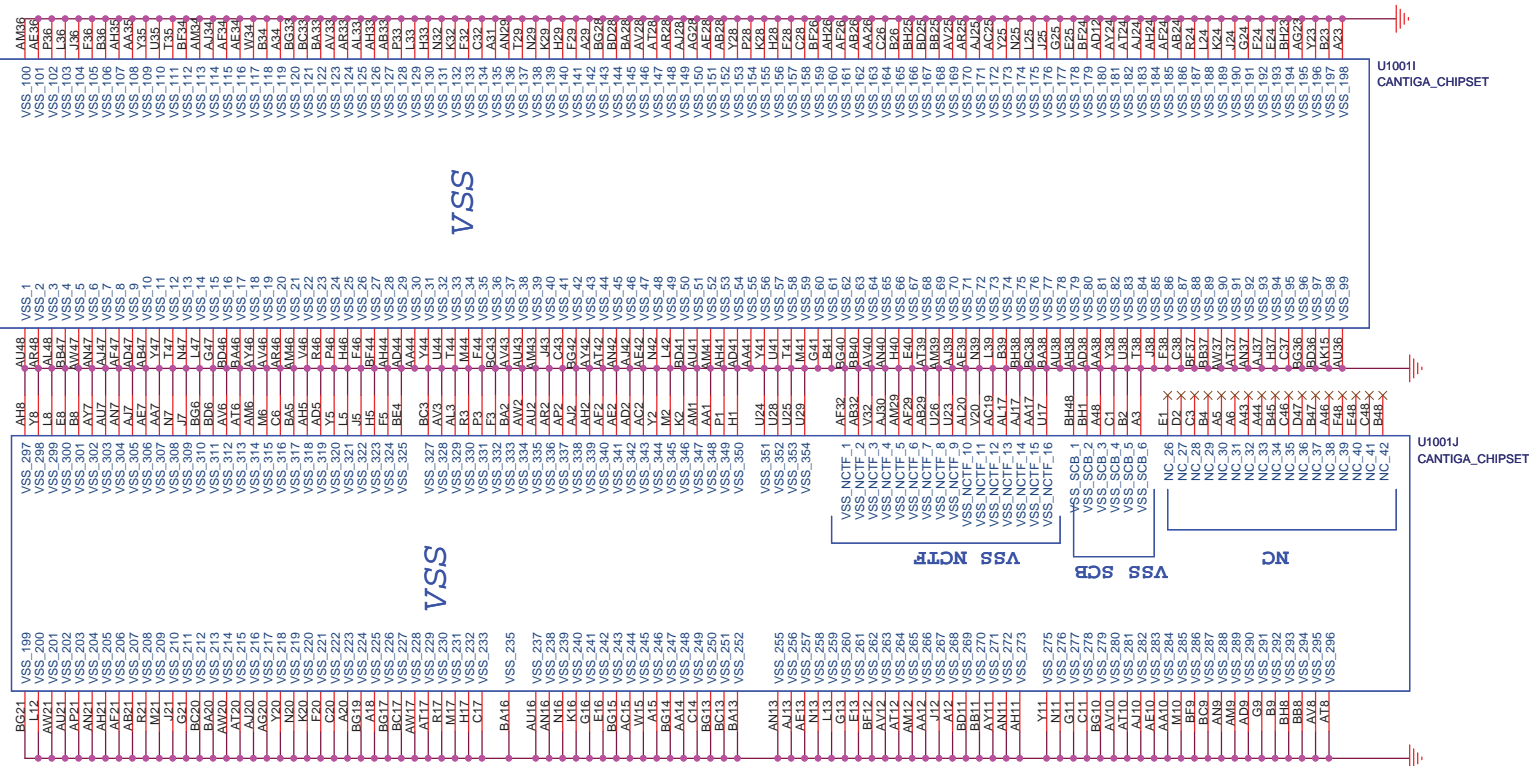


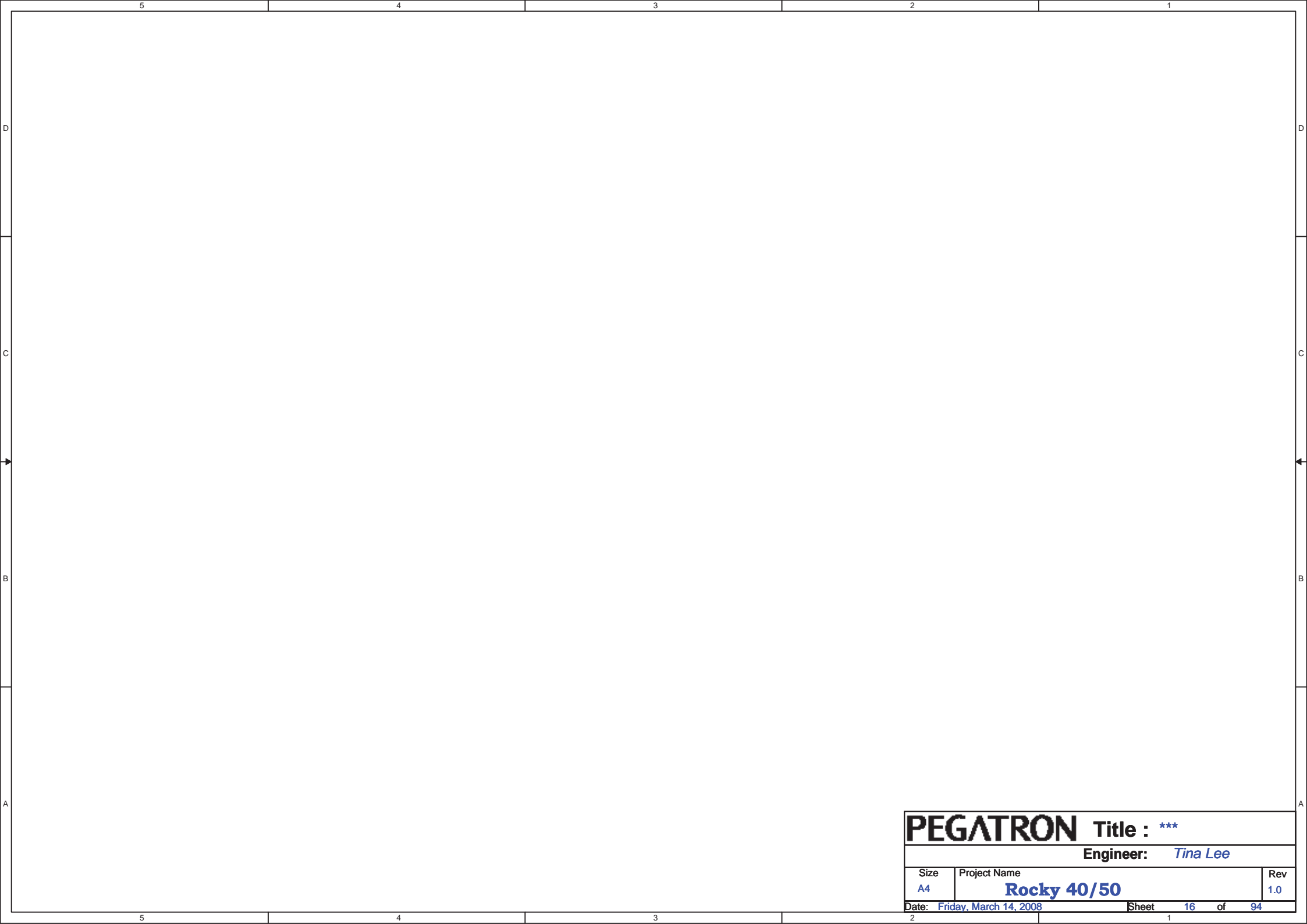










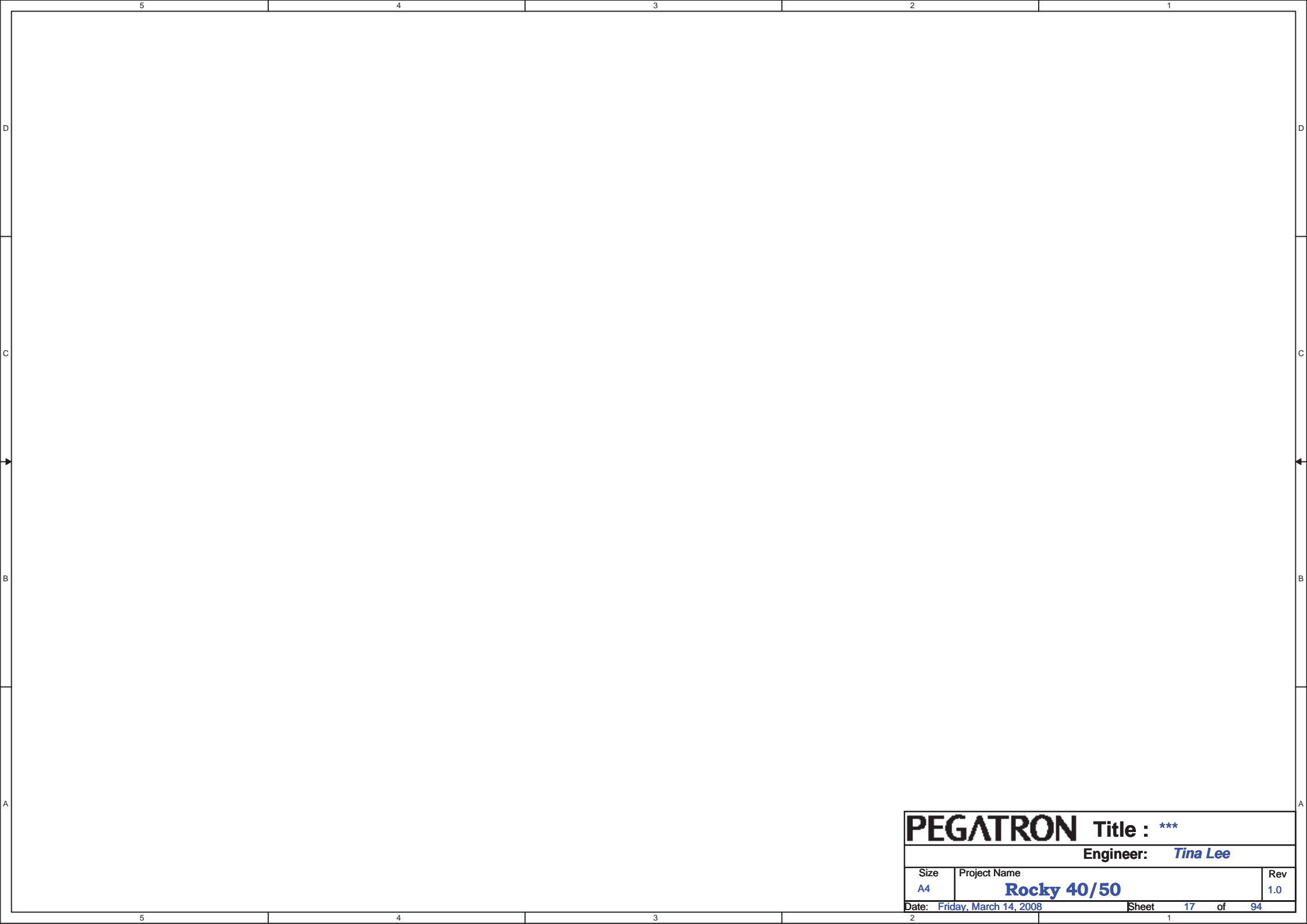


PEGATRON

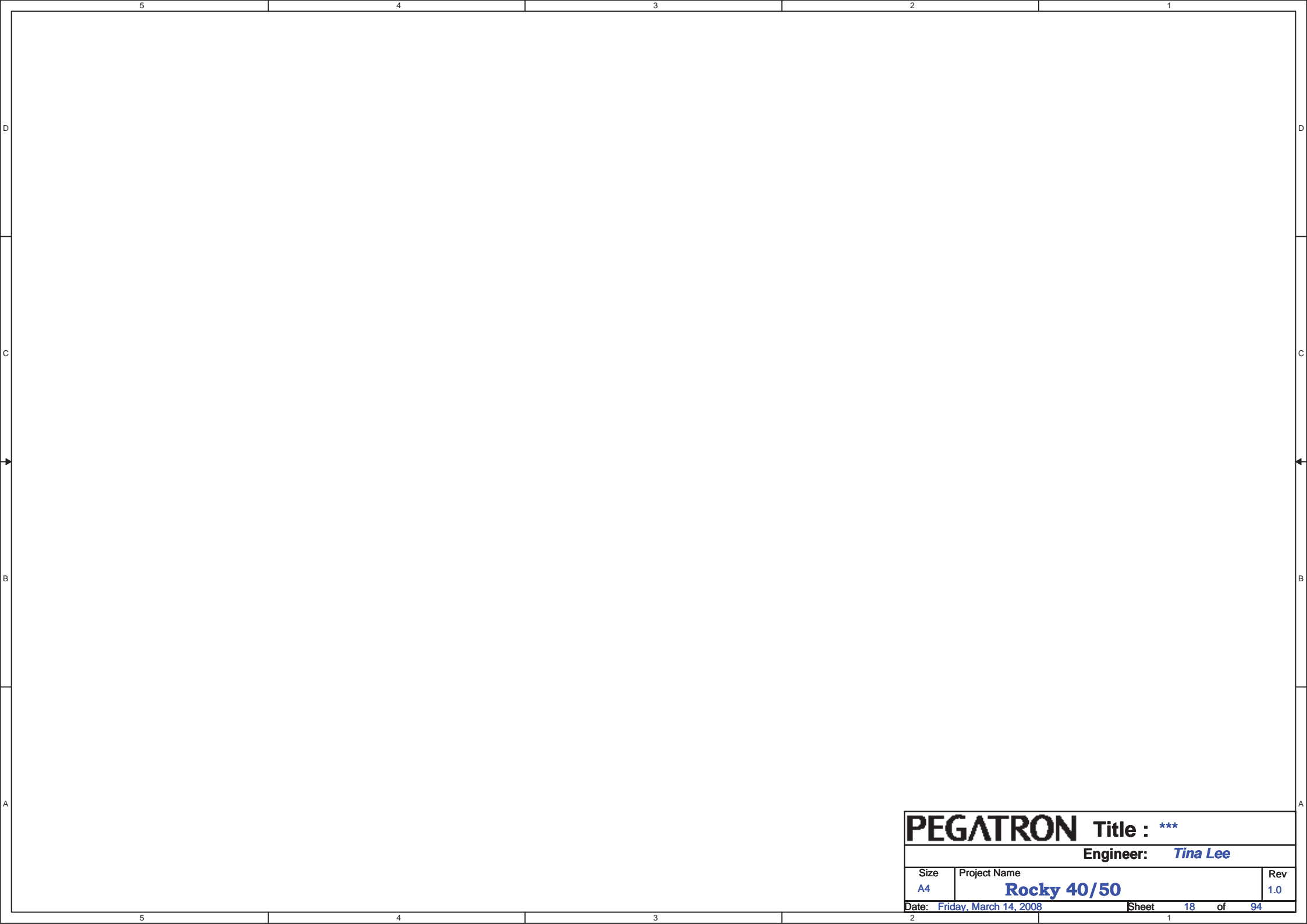
Title : \*\*\*

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 16 of 94	



<b>PEGATRON</b>		Title : ***	
Engineer: Tina Lee			
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet 17 of 94	

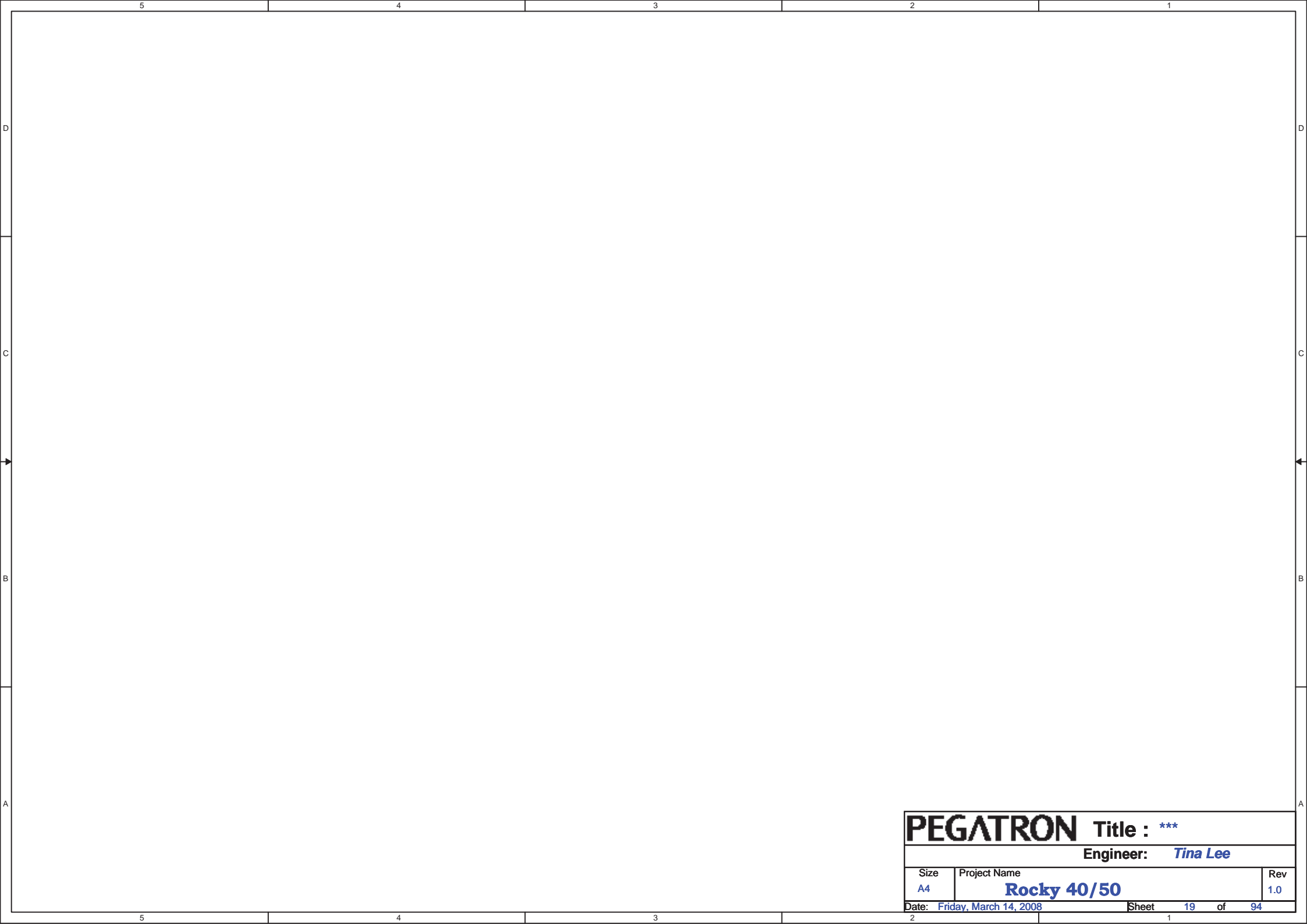


PEGATRON

Title : \*\*\*

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 18 of 94	

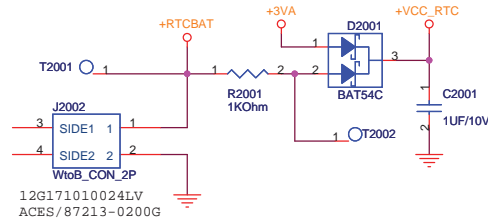
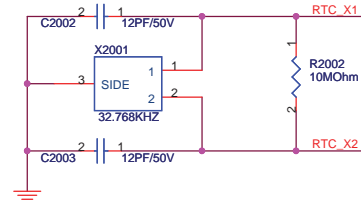
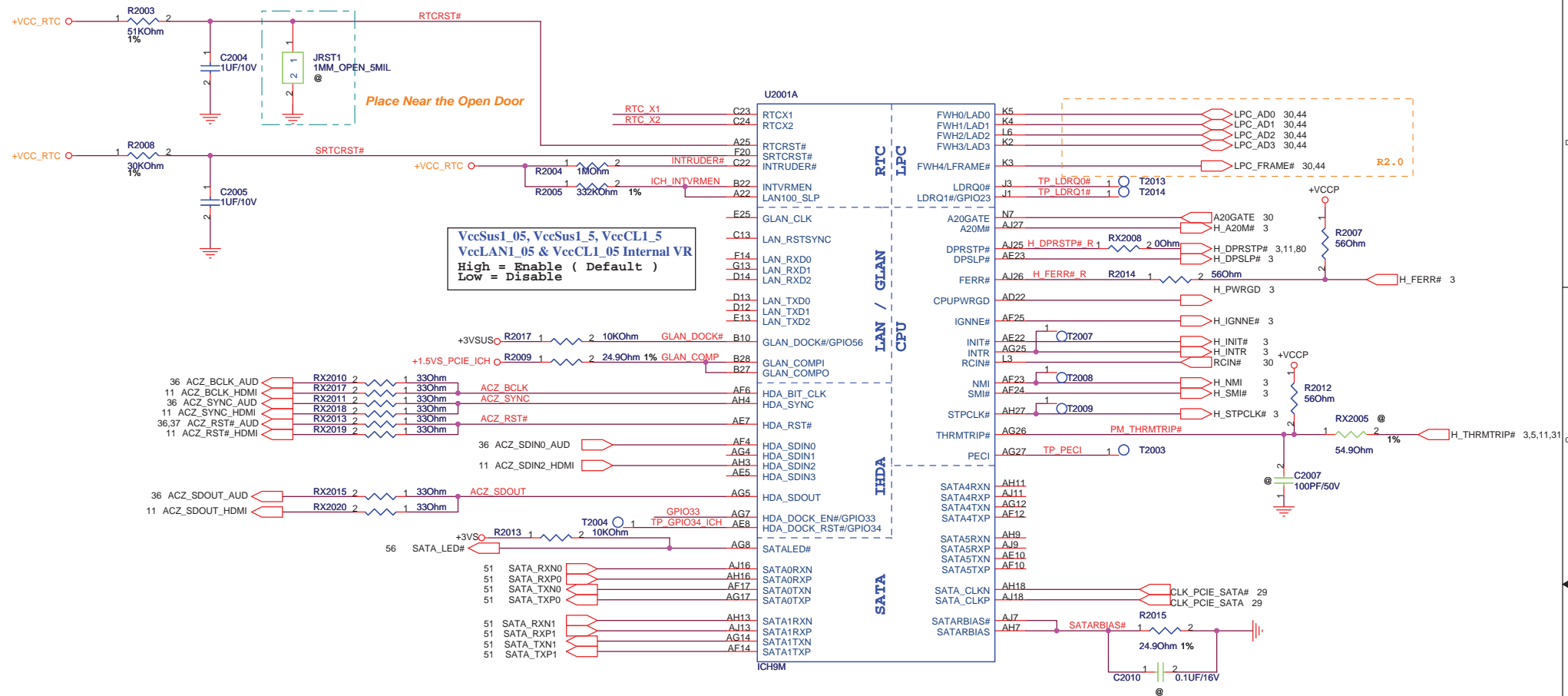


PEGATRON

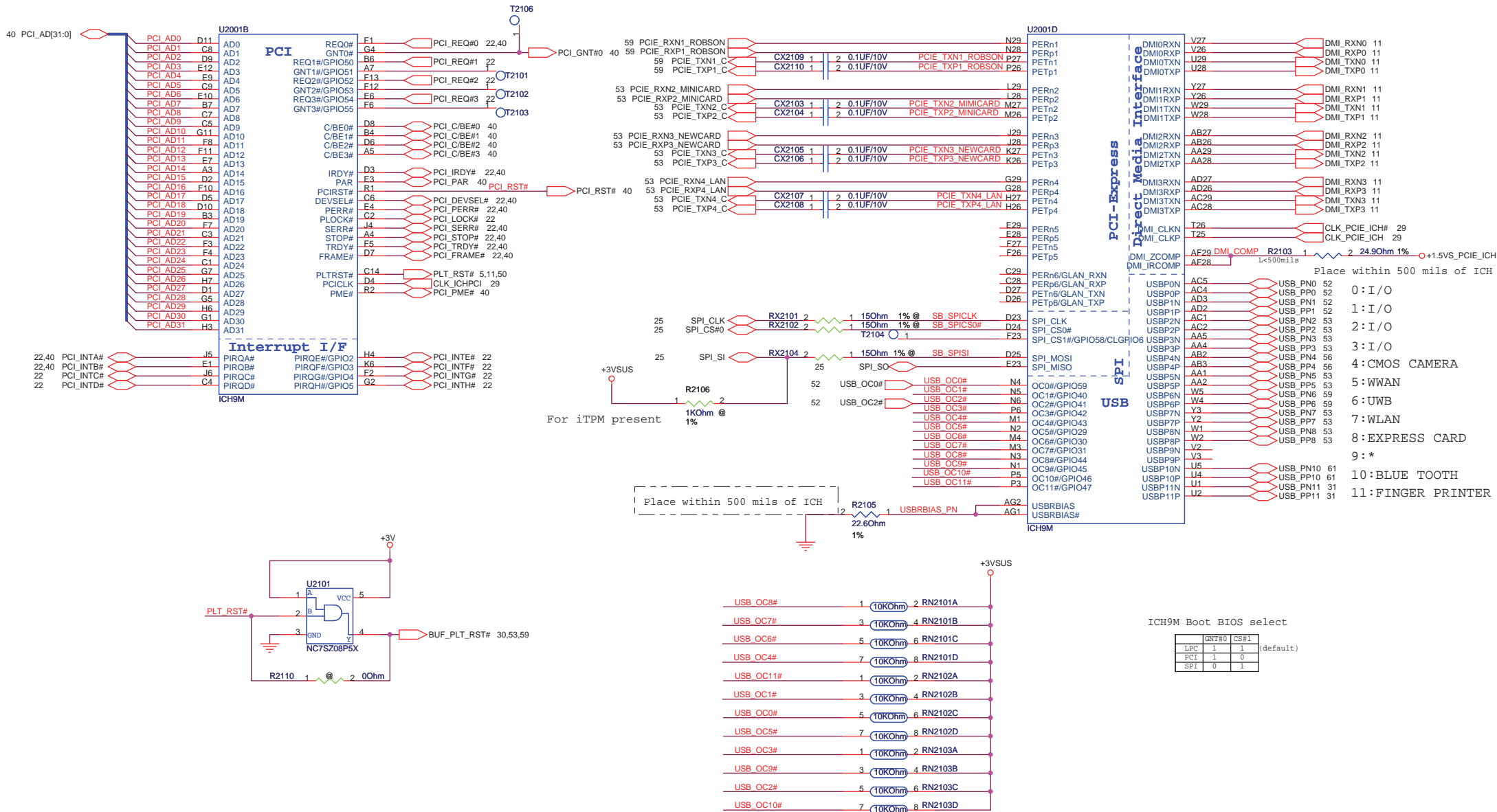
Title : \*\*\*

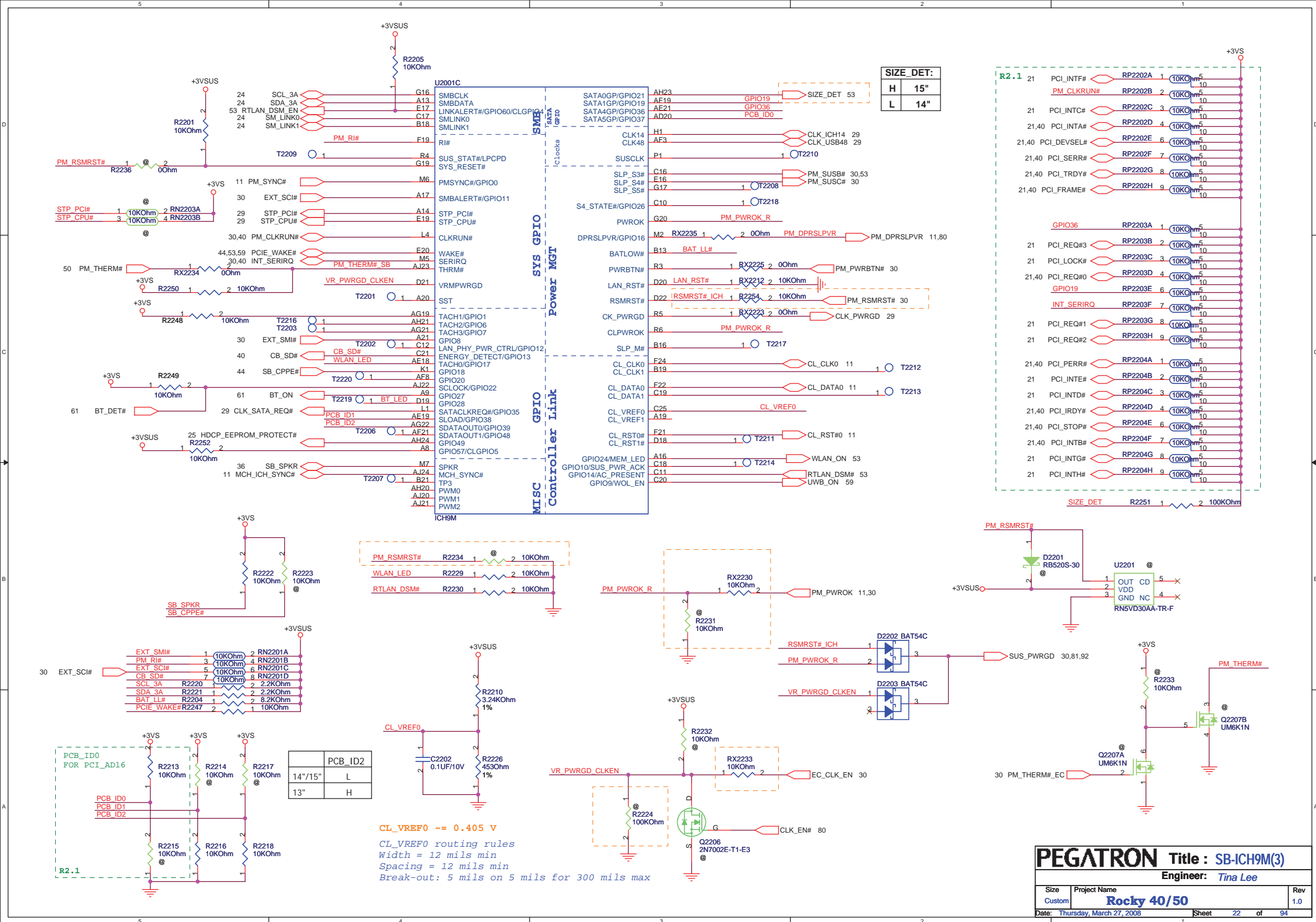
Engineer: Tina Lee

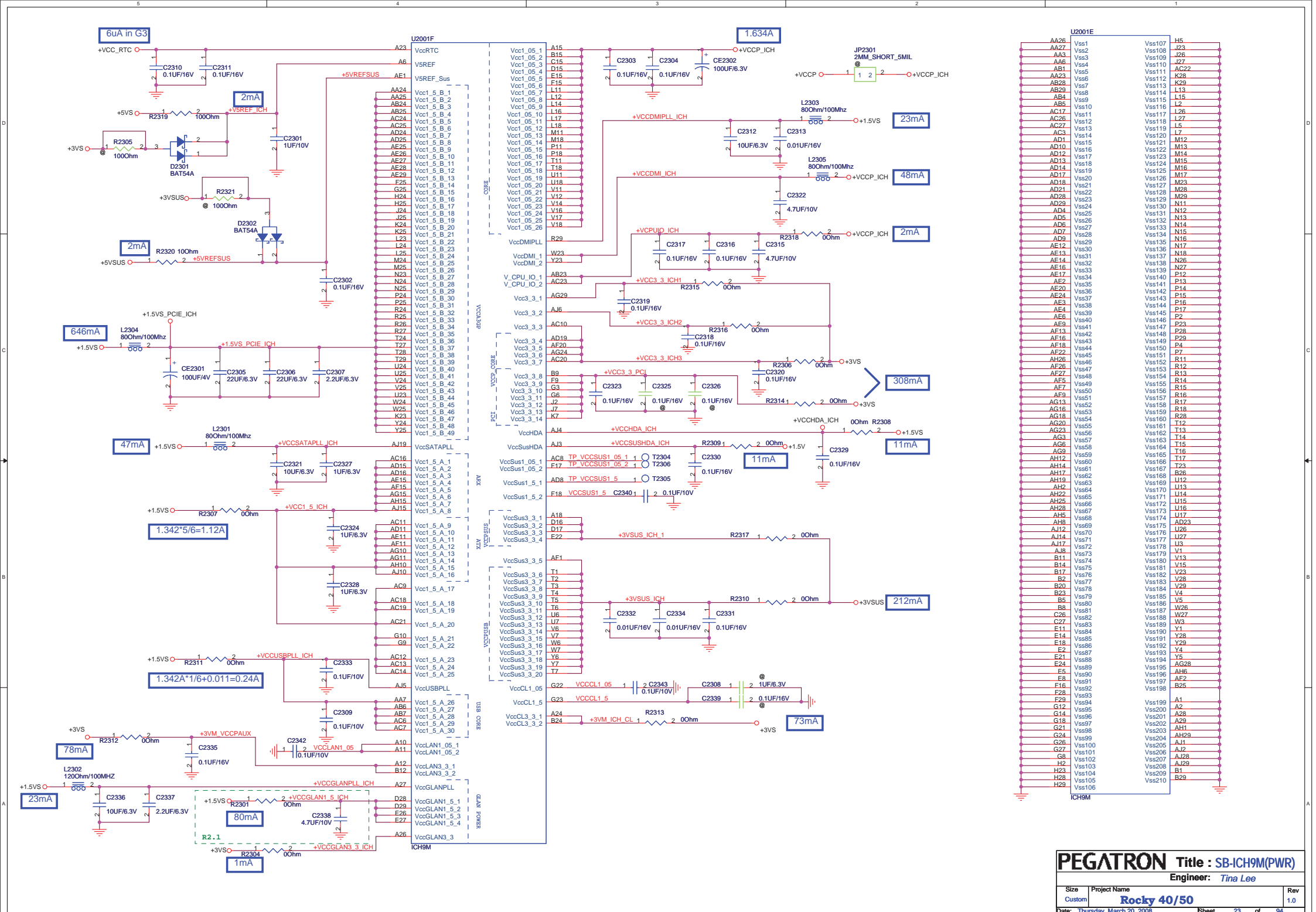
Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 19	of 94



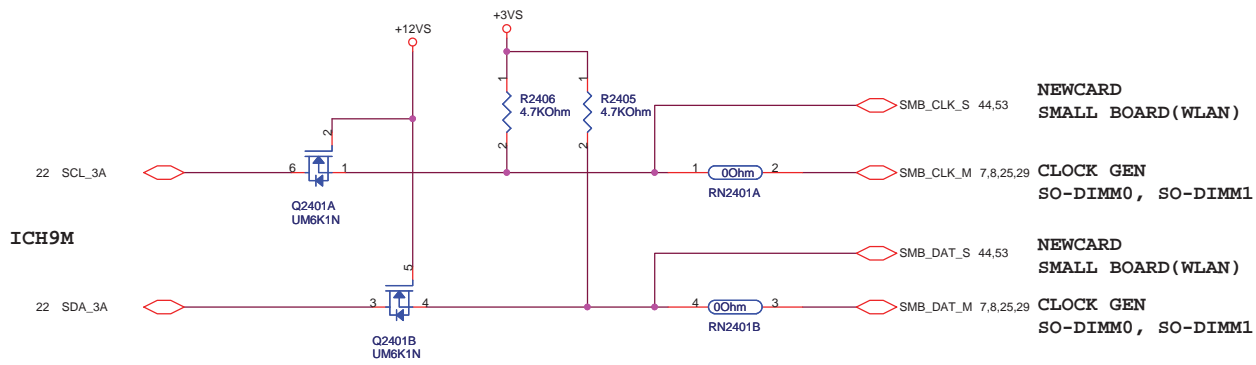
[ICH\_TP3, ACZ\_SDOUT] : XOR Chain Entrance Strap  
 00 = Reserved  
 01 = Enter XOR Chain  
 10 = Normal Operation (Default)  
 11 = Set PCIe Port Config Bit 1



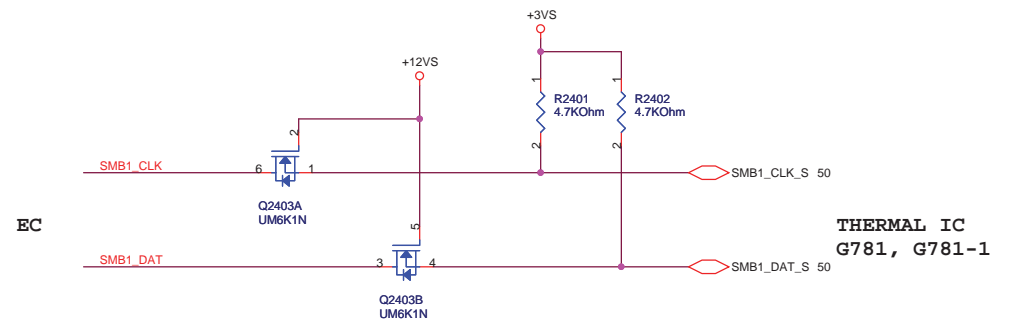
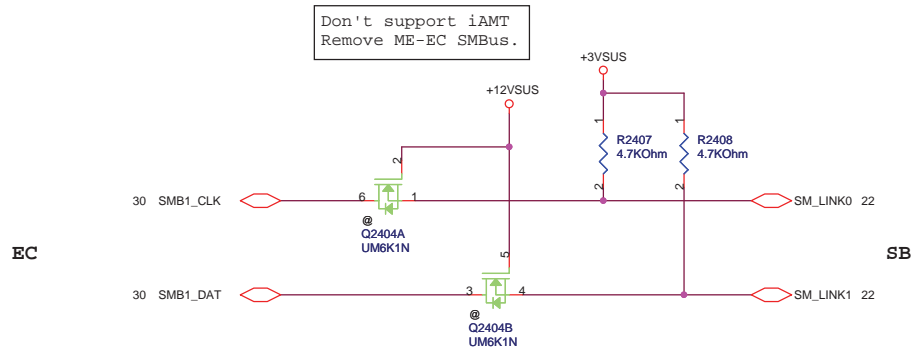


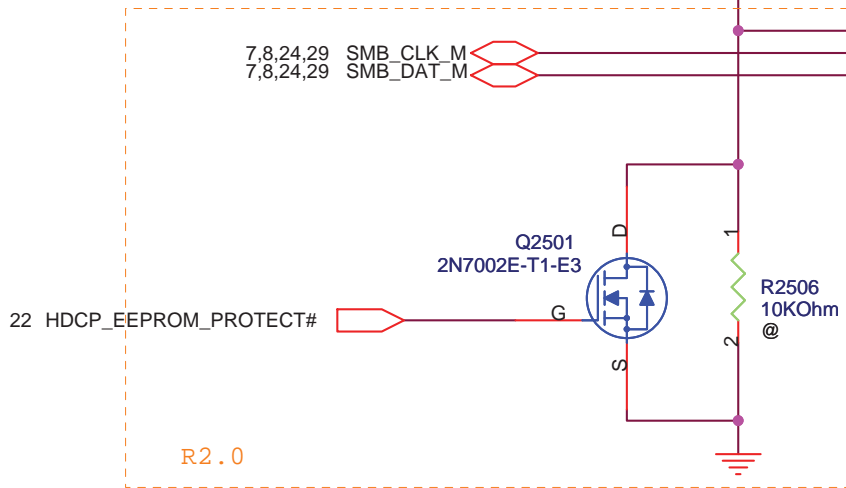
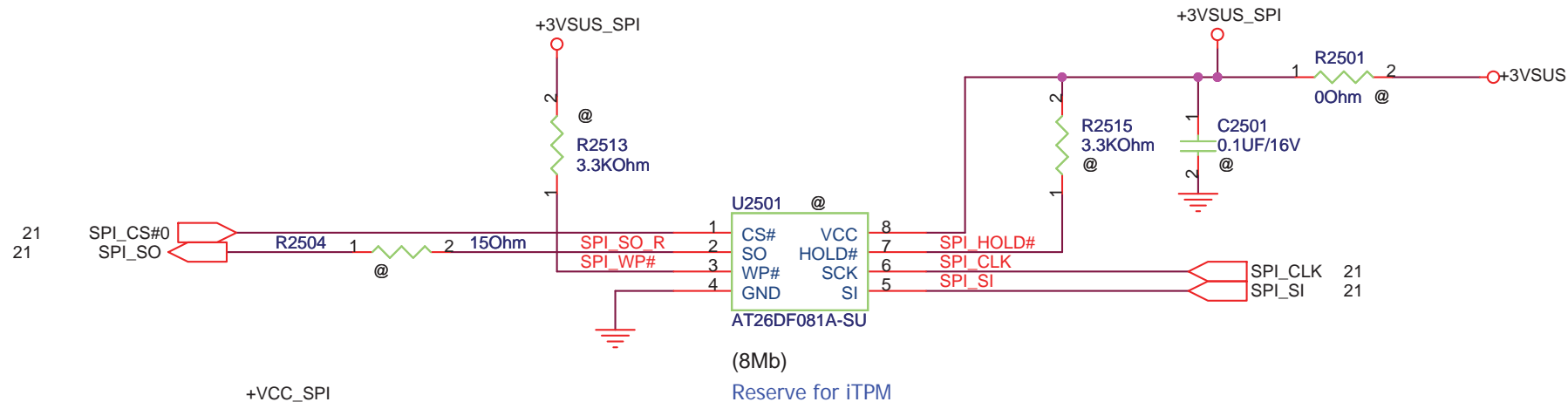


ICH9-M



EC

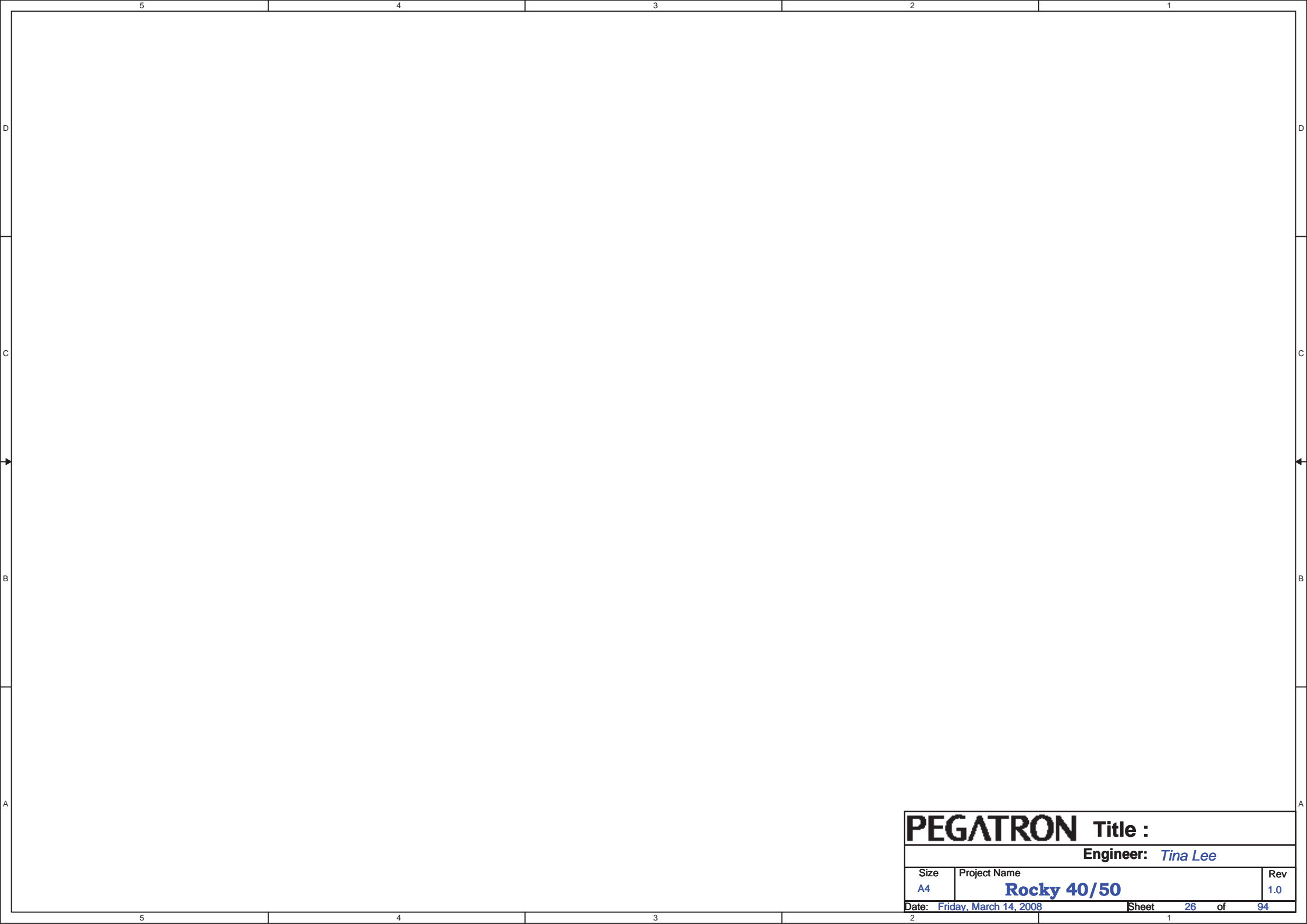




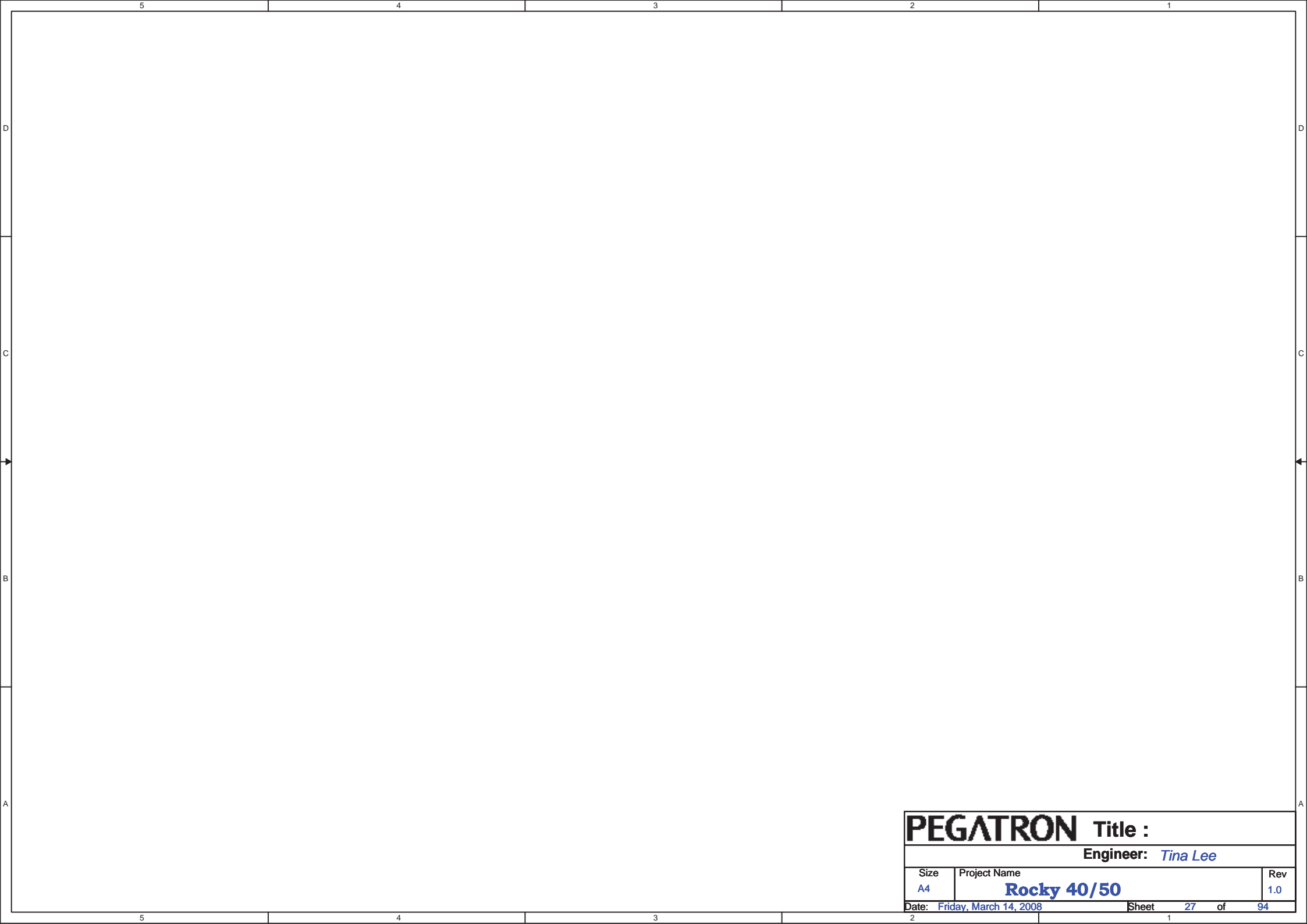
U2502-AT24C08A :  
 Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509  
 Nostuff : R2505

U2503-AT88SC0808C :  
 Stuff : U2503  
 Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

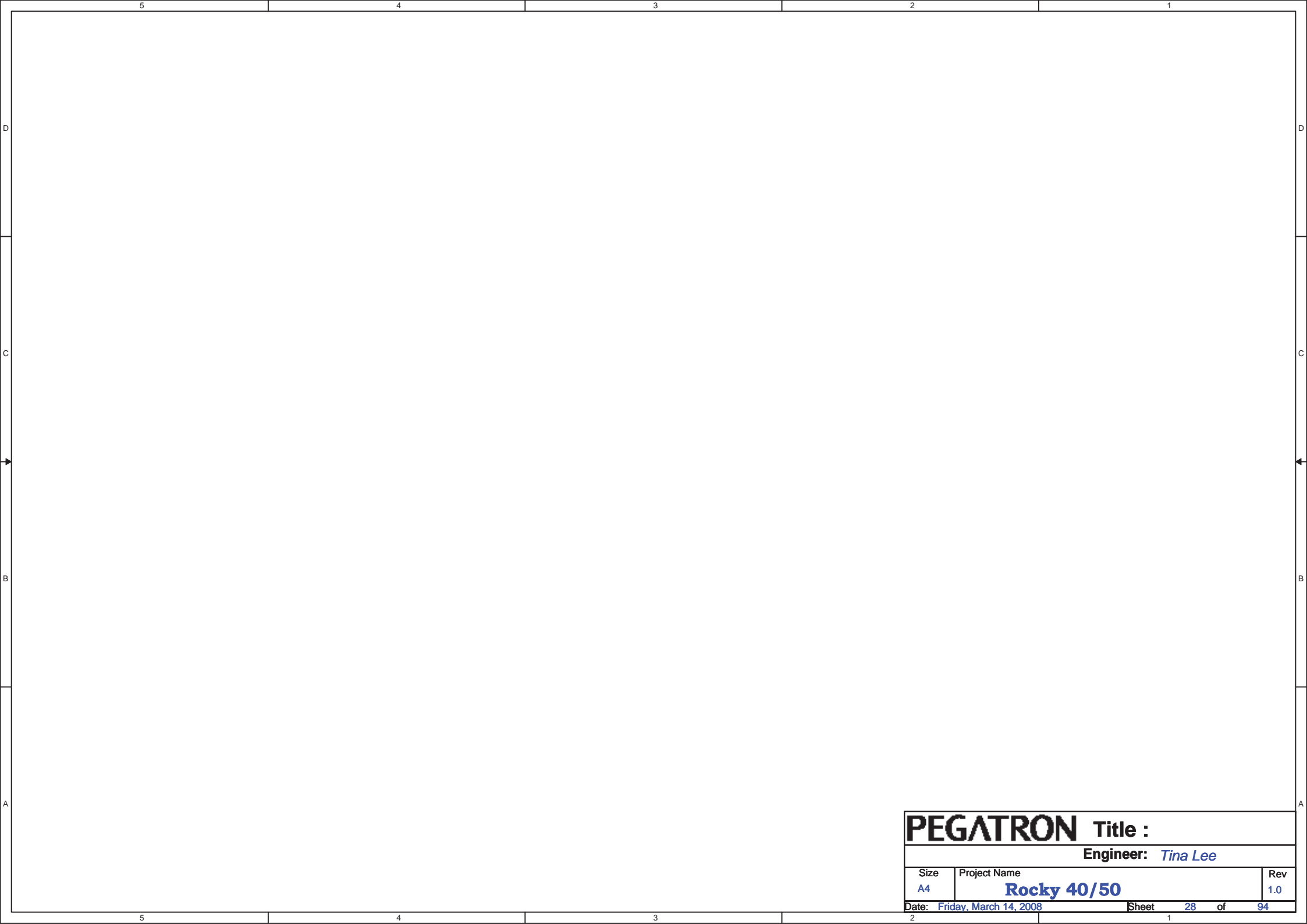
PEGATRON			Title : SPI ROM	
			Engineer: Tina Lee	
Size	Project Name			Rev
Custom	Rocky 40/50			1.0
Date: Thursday, March 27, 2008		Sheet 25 of 94		



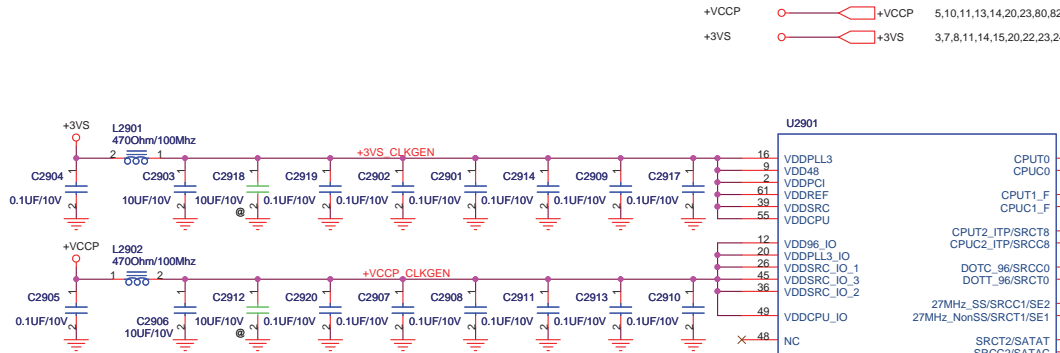
PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	26	of 94



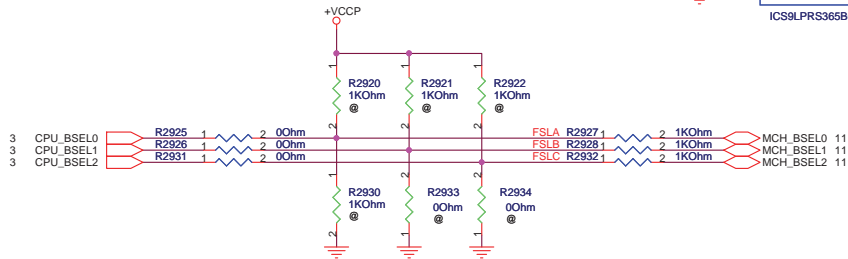
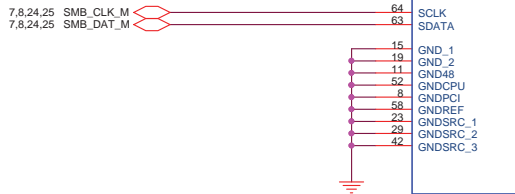
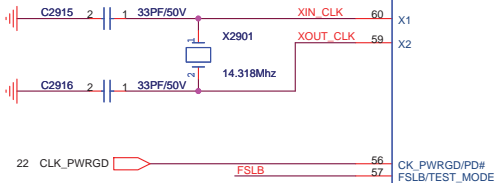
PEGATRON			Title :			
			Engineer: Tina Lee			
Size	Project Name				Rev	
A4	Rocky 40/50				1.0	
Date: Friday, March 14, 2008			Sheet	27	of	94



PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	28	of 94

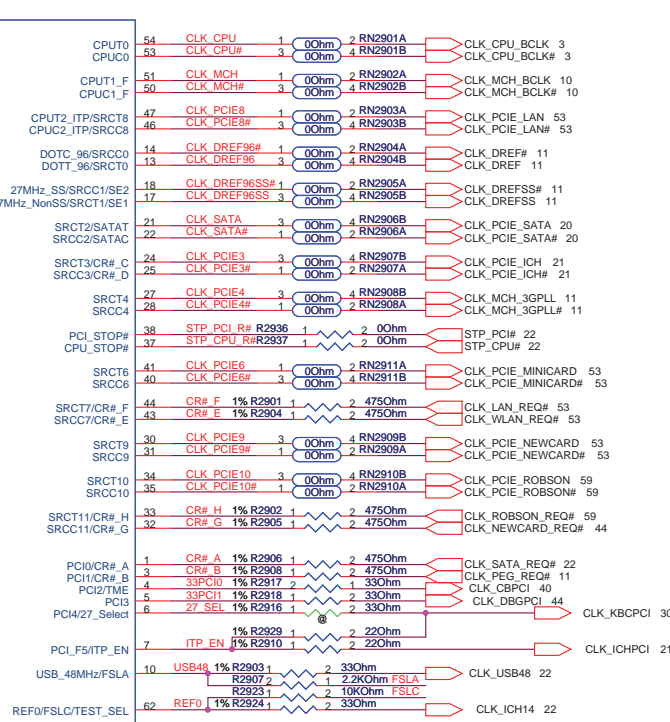


C2917, C2918, C2919 near CLK Gen.

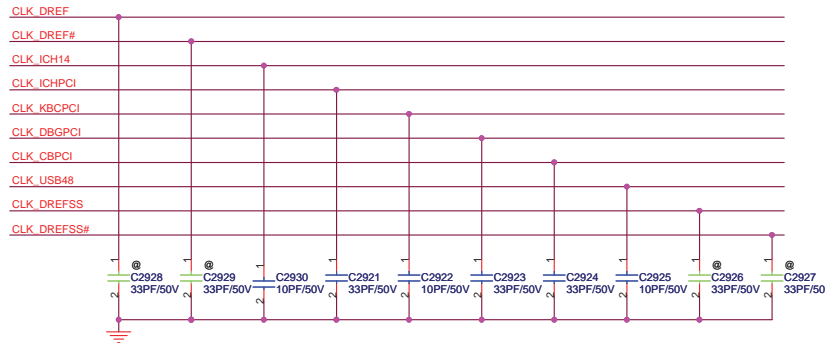


BCLK	FSB	FSLC	FSLB	FSLA
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

+VCCP 5,10,11,13,14,20,23,80,82  
+3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,37,40,41,45,46,48,50,51,53,56,57,58,59,61,91,92



C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.



CR#_A	0 = SRC 0	
CR#_B	1 = SRC 2	SATA
CR#_C	0 = SRC 0	
CR#_D	1 = SRC 1	MCH
CR#_E	SRC 6	WLAN
CR#_F	SRC 8	LAN
CR#_G	SRC 9	New Card
CR#_H	SRC 10	Robson

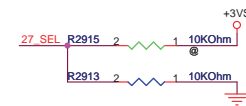
## Latched Input Select

0 = SRC 8 Decide pin  
1 = CPU\_ITP CLK 46, 47



27\_Select=0, Decide pin  
pin#13/14=DOT96; 13/14,17/18  
pin#17/18=LCD\_SST;

27\_Select=1, Decide pin  
pin#13/14=SRC0; 13/14,17/18  
pin#17/18=27MHz non-spread SE clock;



For GM/GL, need to PD for 96MHz output.  
For PM, need to PU for 27MHz output.

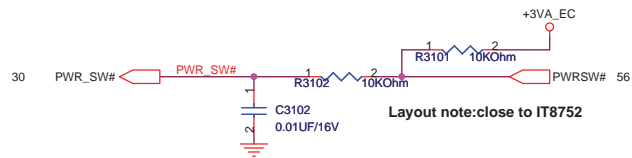
PEGATRON Title : ICS9LPR365  
Engineer: Tina Lee

Size Project Name  
Custom Rocky 40/50  
Date: Thursday, March 27, 2008 Sheet 29 of 94



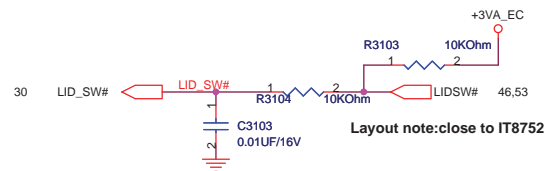
### For Switch

PWR  
SWITCH

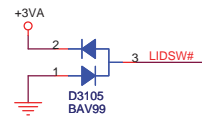


Layout note:close to IT8752

LID  
SWITCH



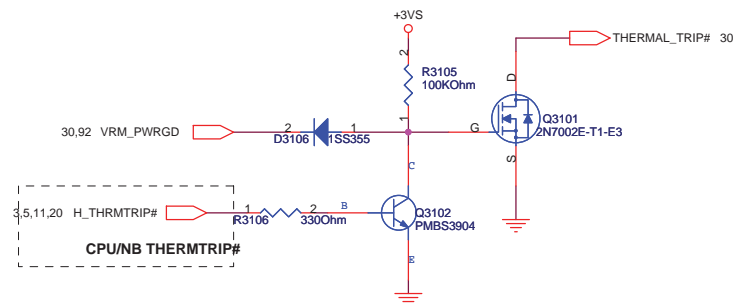
Layout note:close to IT8752



**close to connector**

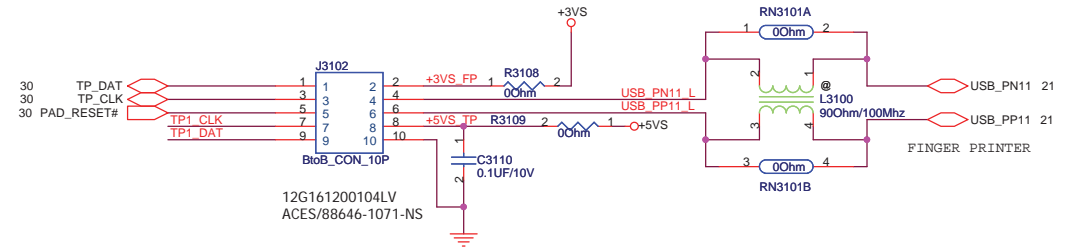
Note:  
LID\_SW# is easy to cause high voltage damage when  
plugging inverter board connector to M/B with AC present.  
Need to add bidirectional diode to protect this pin.

### For Thermal Control Method



CPU/NB THERMTRIP#

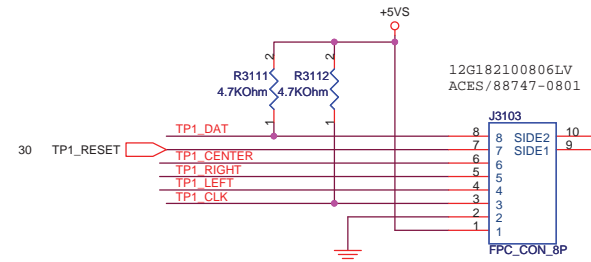
## TOUCH PAD CONN



12G161200104LV  
ACES/88646-1071-NS

TP :Touch Pad  
TP1:Trach Point

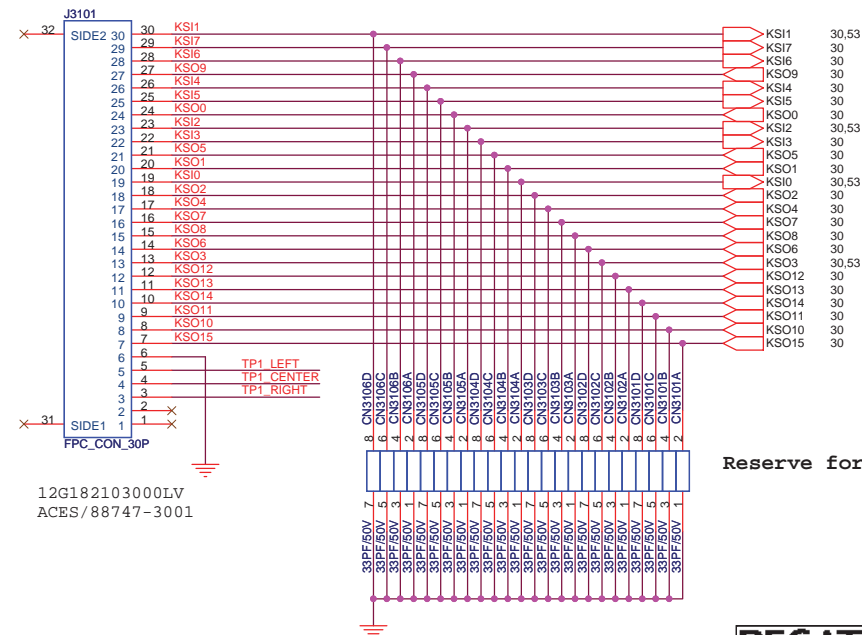
## TRACK POINT CONN



12G182100806LV  
ACES/88747-0801

FPC\_CON\_8F

## Keyboard Connector



Reserve for WWAN

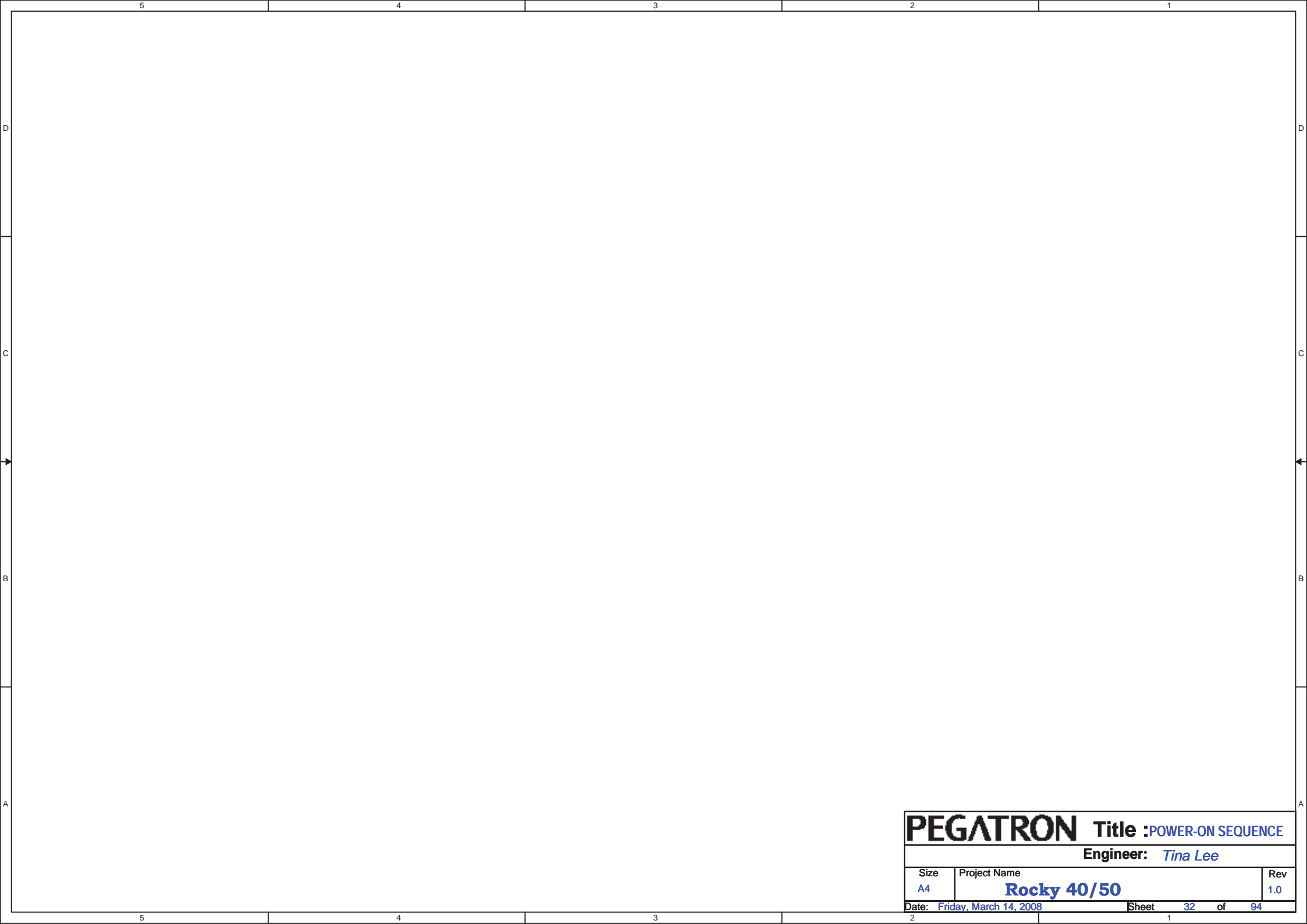
12G182103000LV  
ACES/88747-3001

PFGATRON Title : EC\_IT8752 (2/2)

Engineer: *Tina Lee*

Size Custom	Project Name <b>Rocky 40/50</b>	Rev 1.0
Date: Thursday, March 27, 2008		Sheet 31 of 94

Date: Thursday, March 27, 2008 Sheet 31 of 94

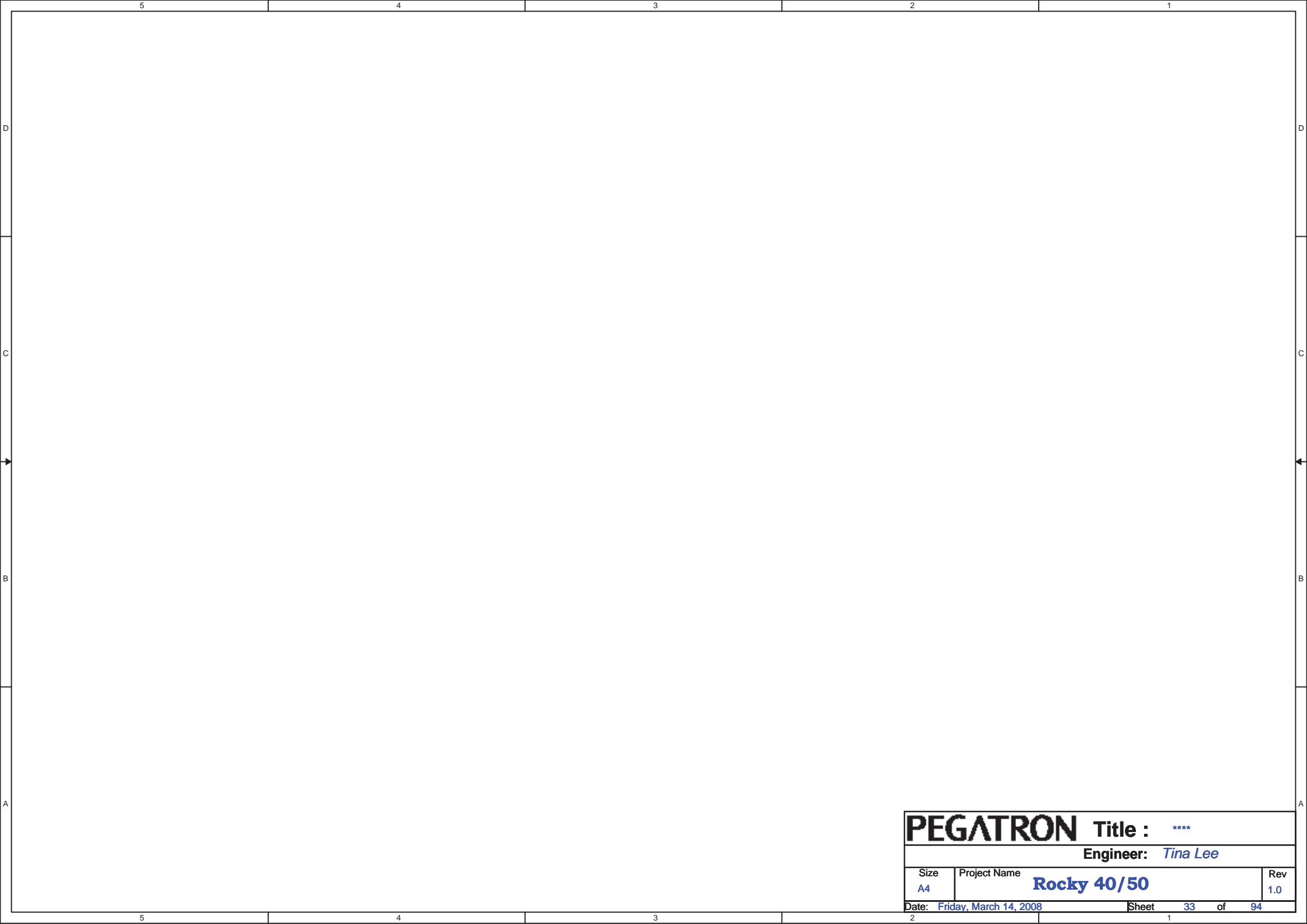


PEGATRON

Title :POWER-ON SEQUENCE

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 32 of 94	

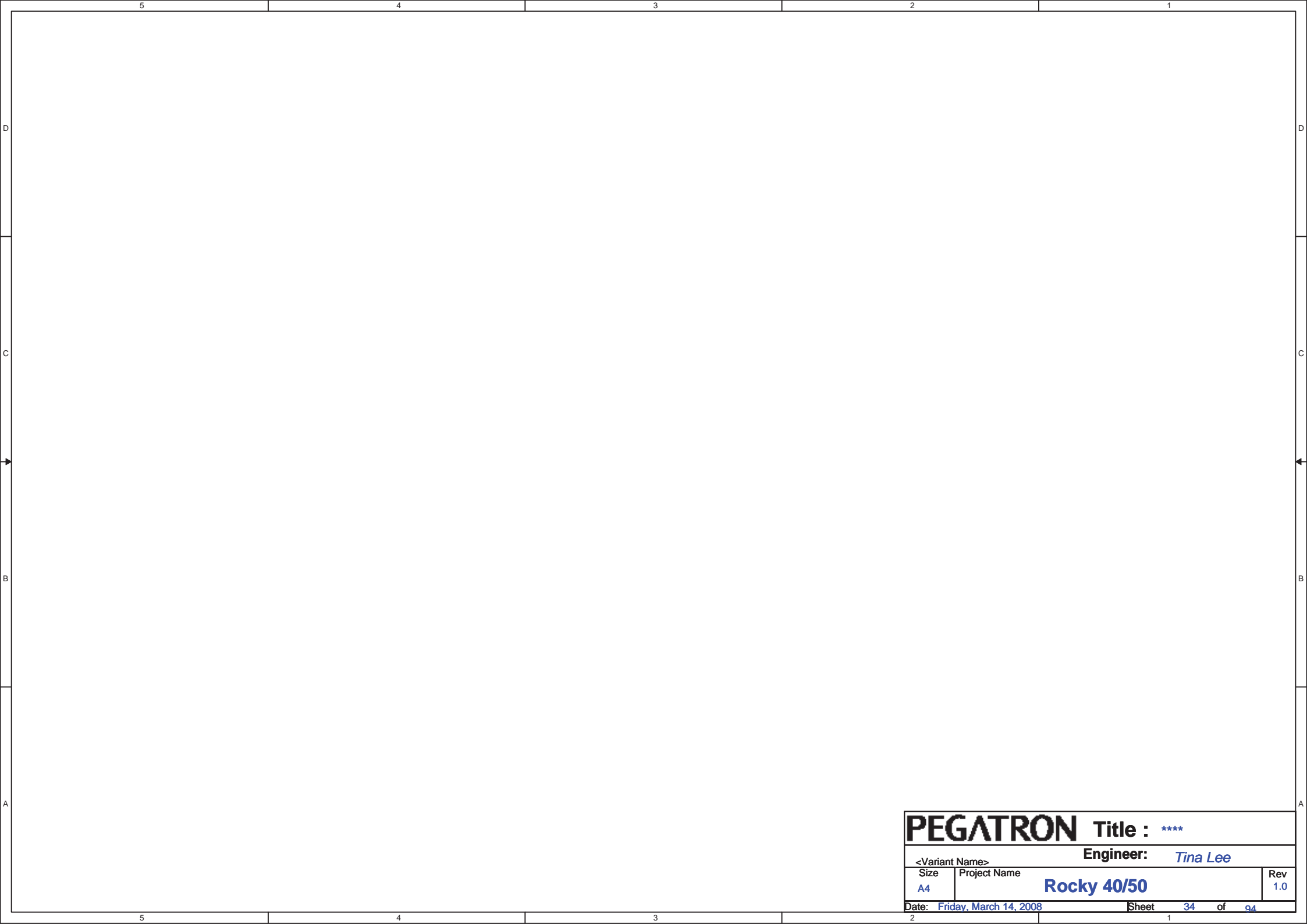


PEGATRON

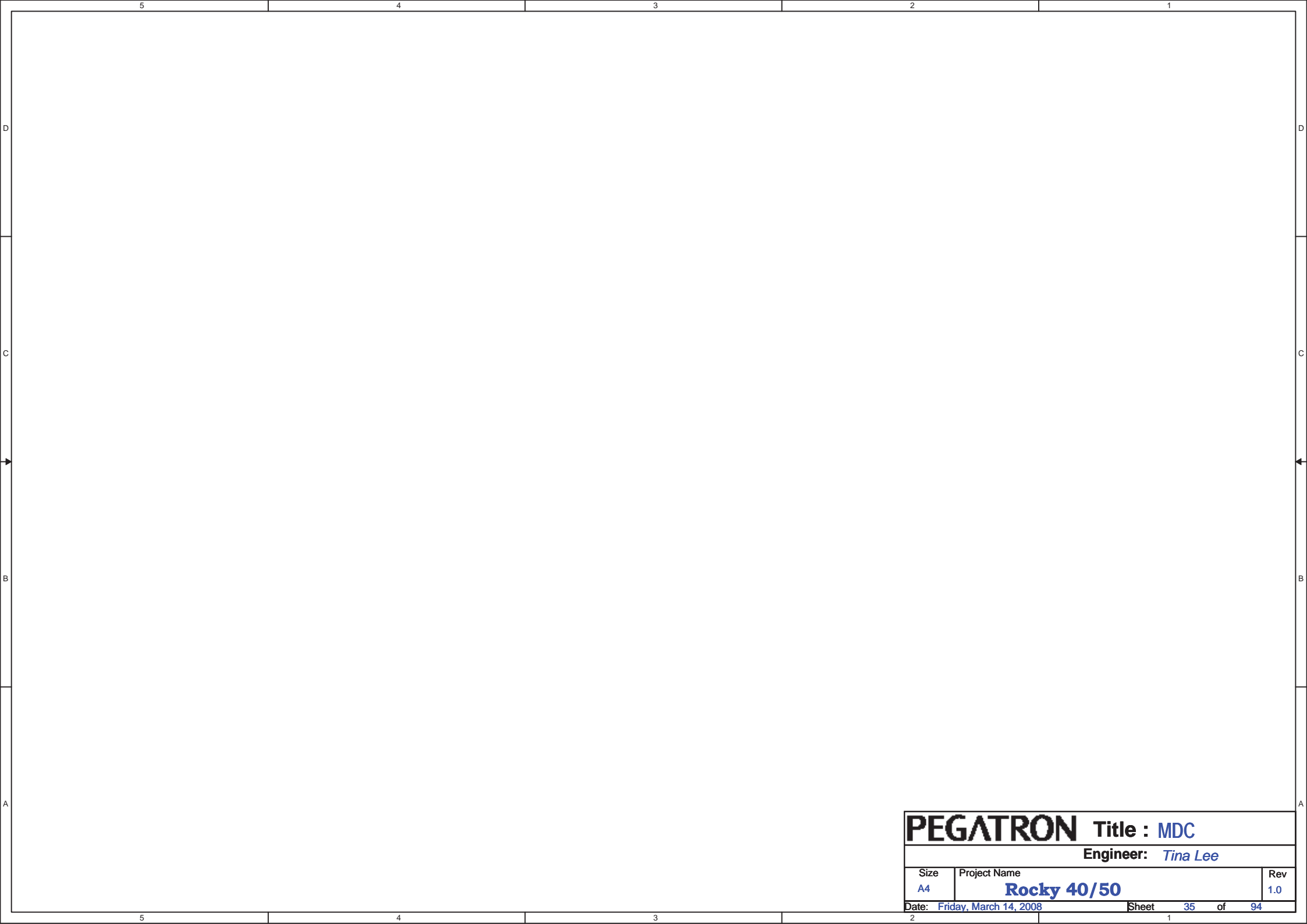
Title : \*\*\*\*\*

Engineer: Tina Lee

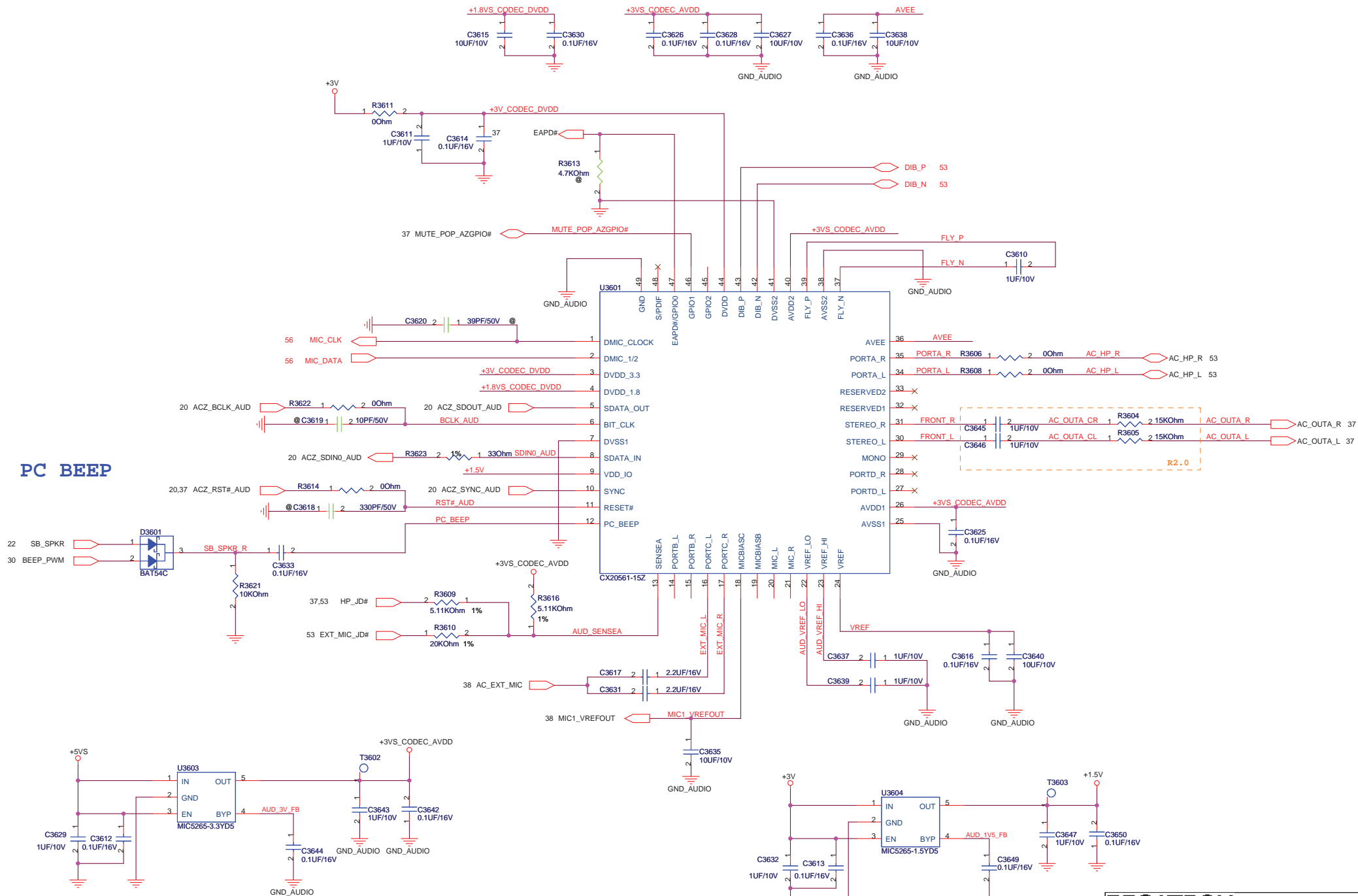
Size A4	Project Name <b>Rocky 40/50</b>	Rev 1.0
Date: Friday, March 14, 2008		Sheet 33 of 94



PEGATRON		Title : ****	
<Variant Name>		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	34 of 94

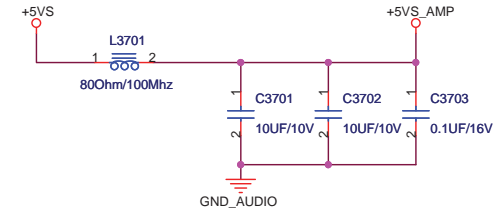
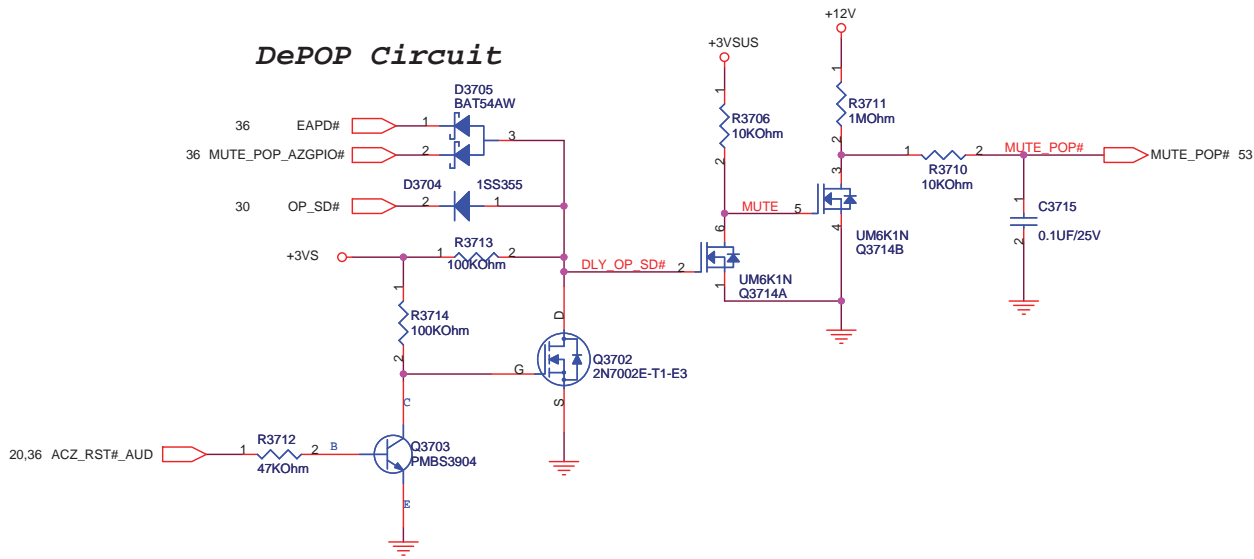


<b>PEGATRON</b>		Title : <b>MDC</b>	
		Engineer: <i>Tina Lee</i>	
Size	Project Name		Rev
<b>A4</b>	<b>Rocky 40/50</b>		<b>1.0</b>
Date:	Friday, March 14, 2008		Sheet 35 of 94

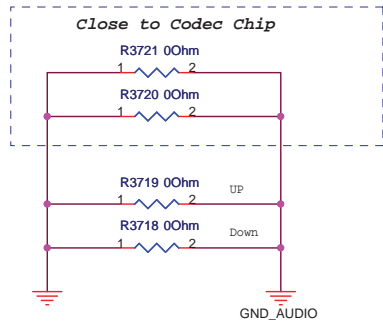


PC BEEP

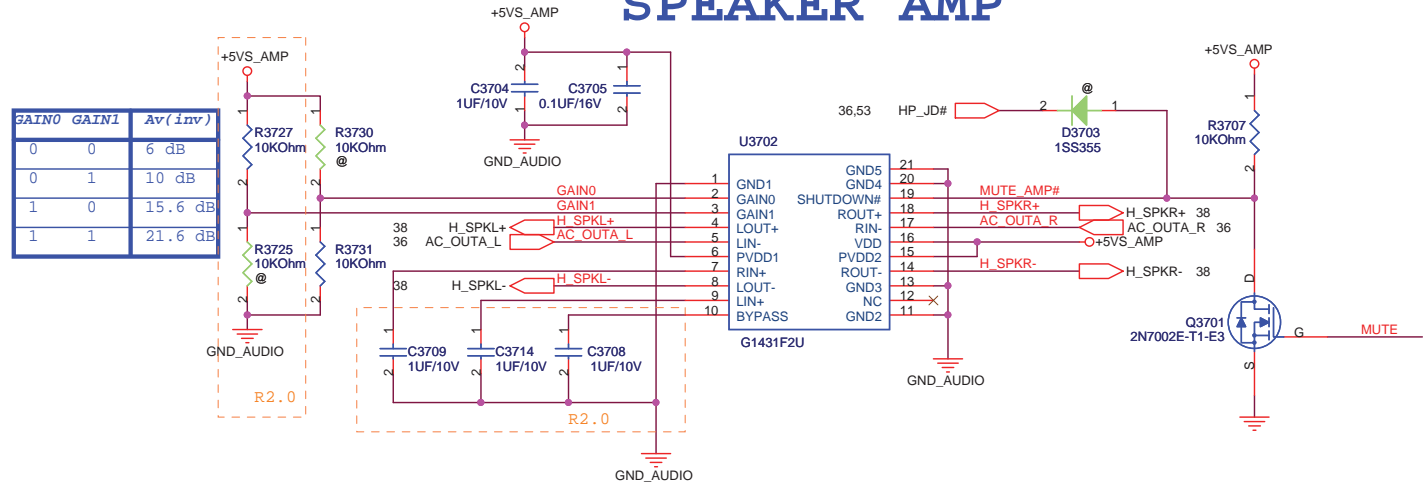
## DePOP Circuit



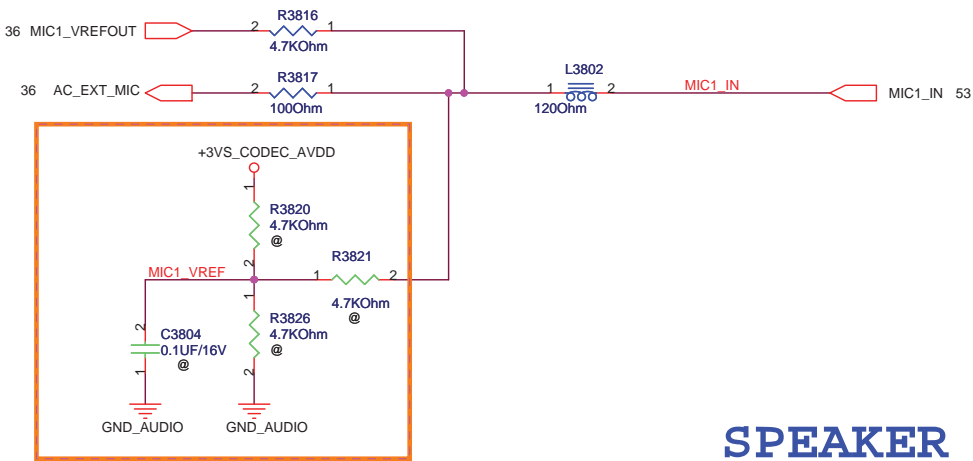
## JACK GND



## SPEAKER AMP

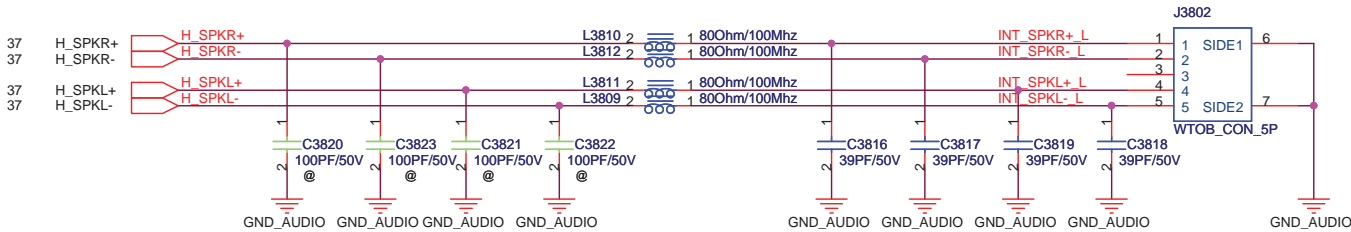


# EXT MICROPHONE

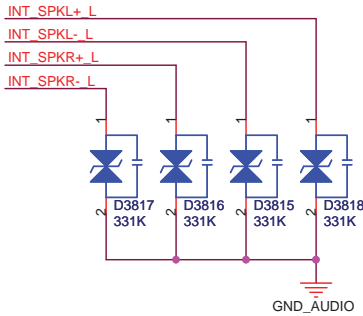


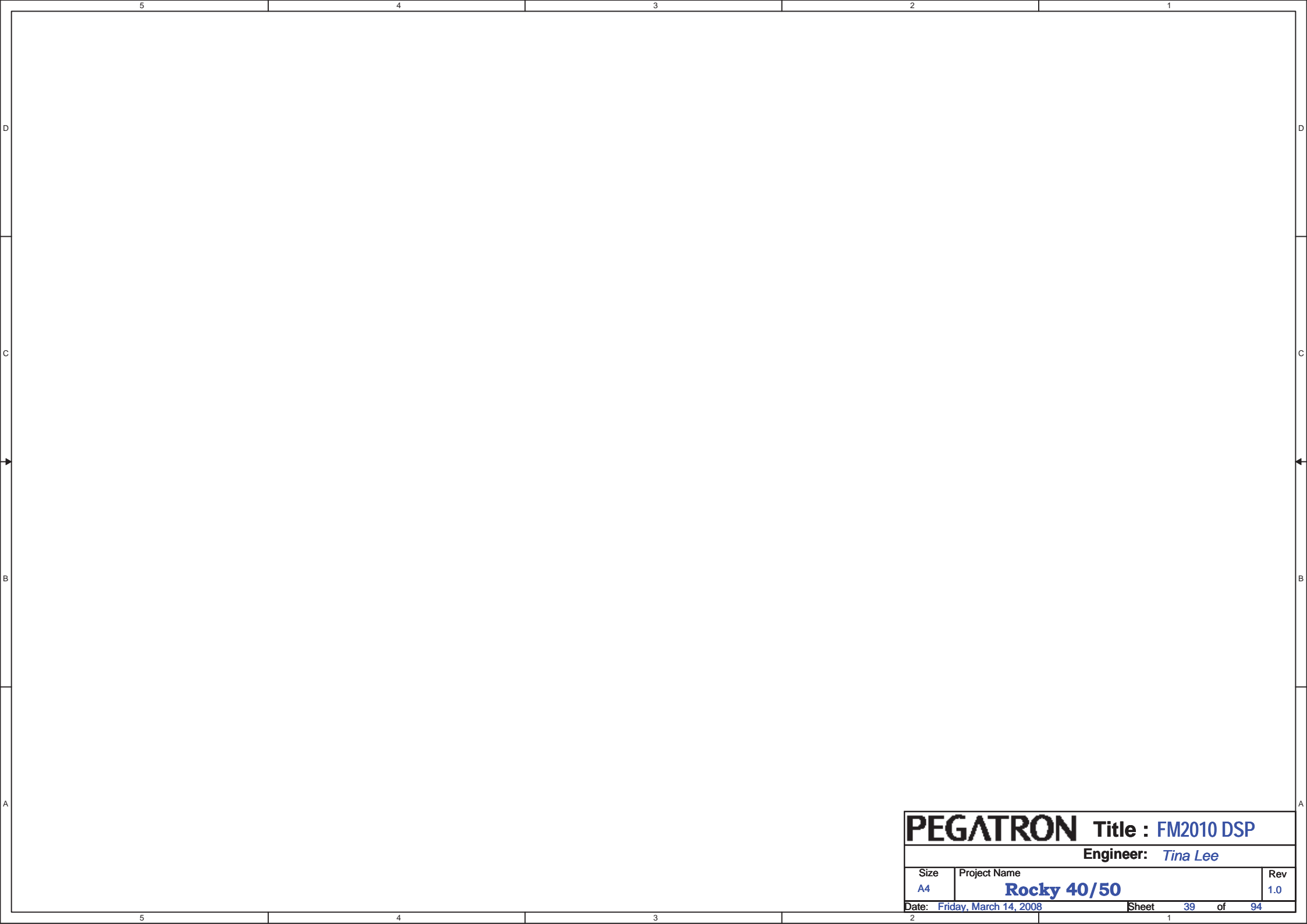
Reserved the external MIC bias(T filter).

# SPEAKER CONNECTOR



12G171010050LV  
ACES/87213-0500G





PEGATRON

Title : FM2010 DSP

Engineer: Tina Lee

Size

A4

Project Name

Rocky 40/50

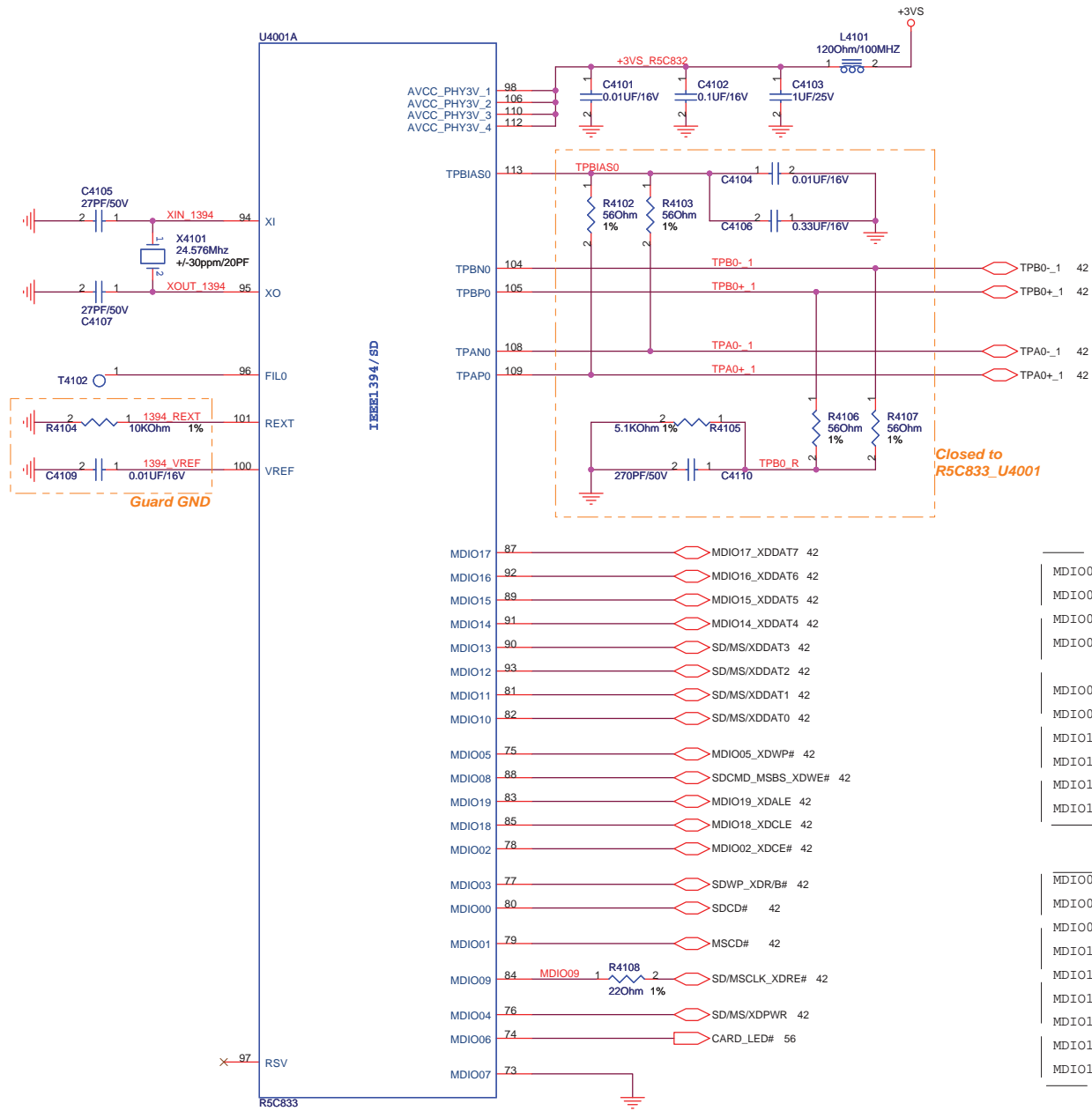
Rev

1.0

Date: Friday, March 14, 2008

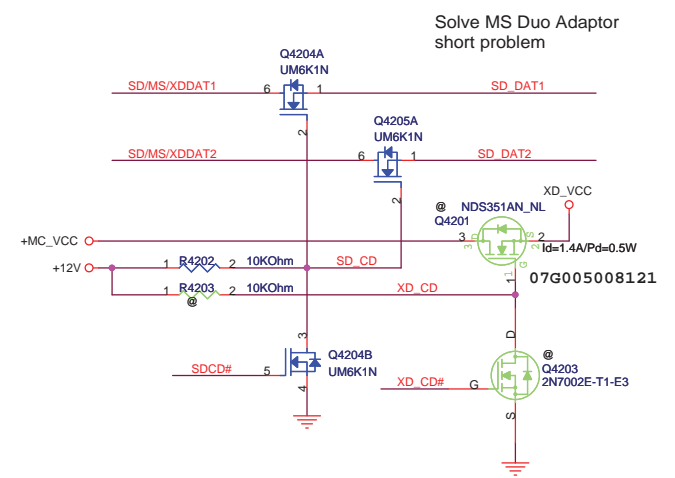
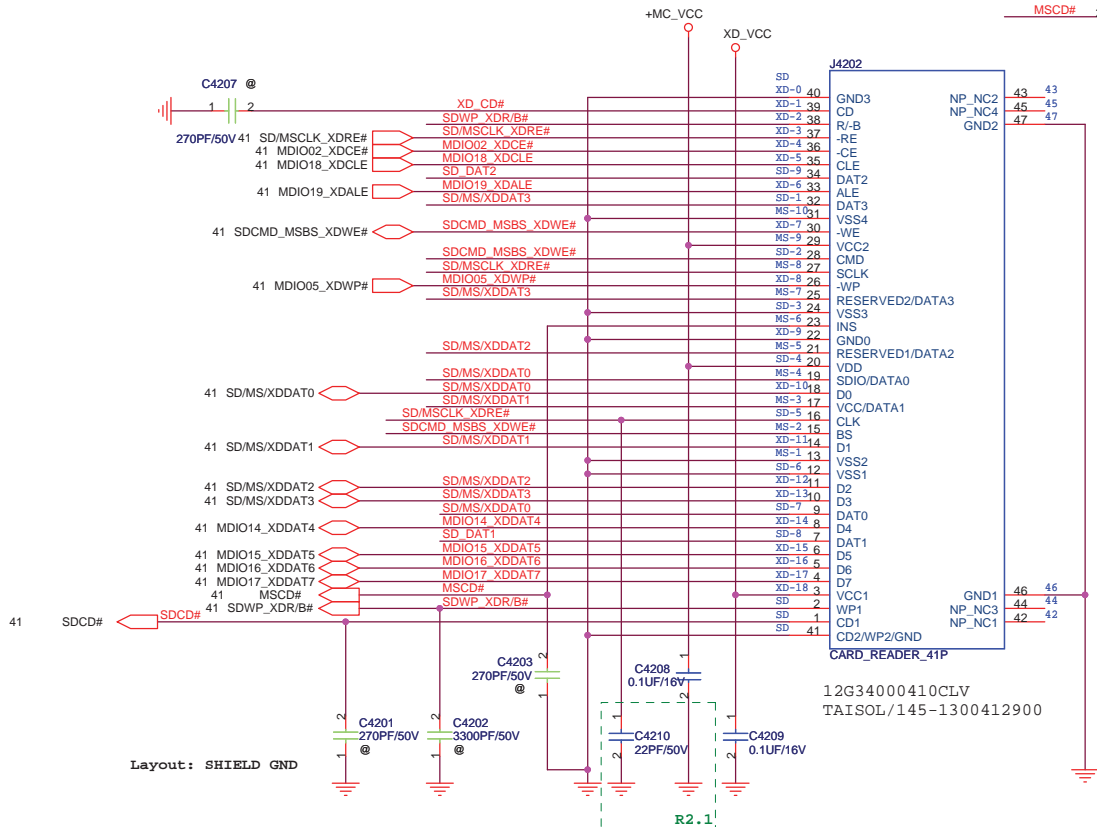
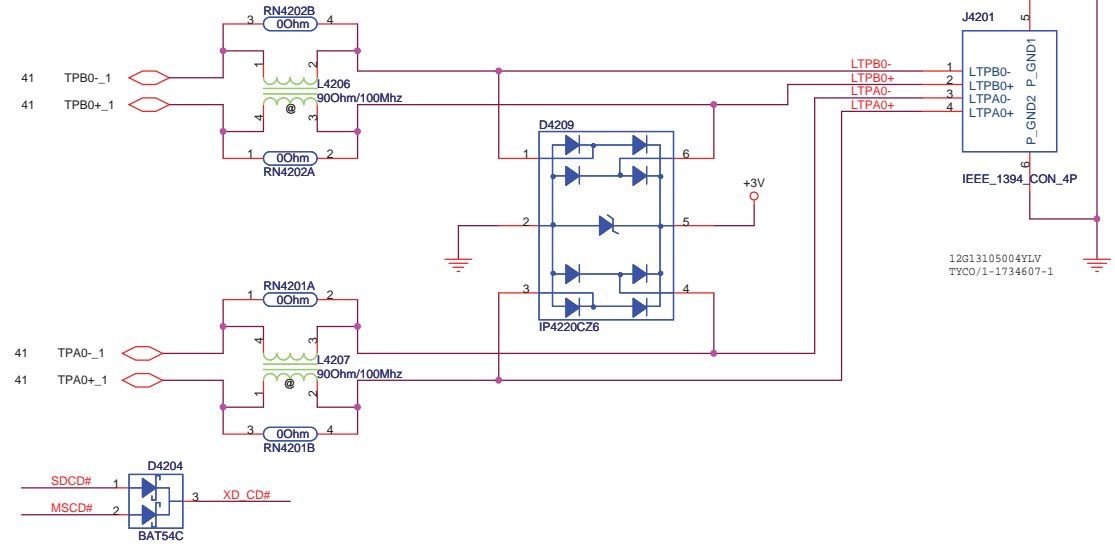
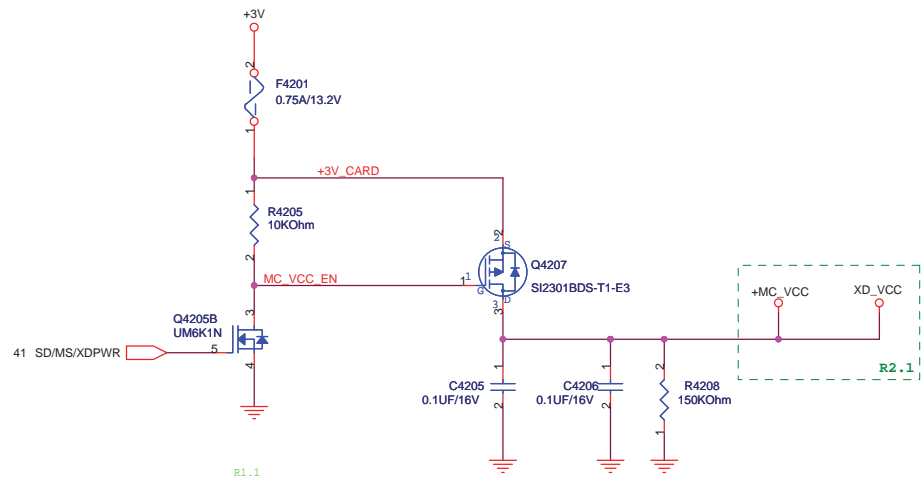
Sheet 39 of 94

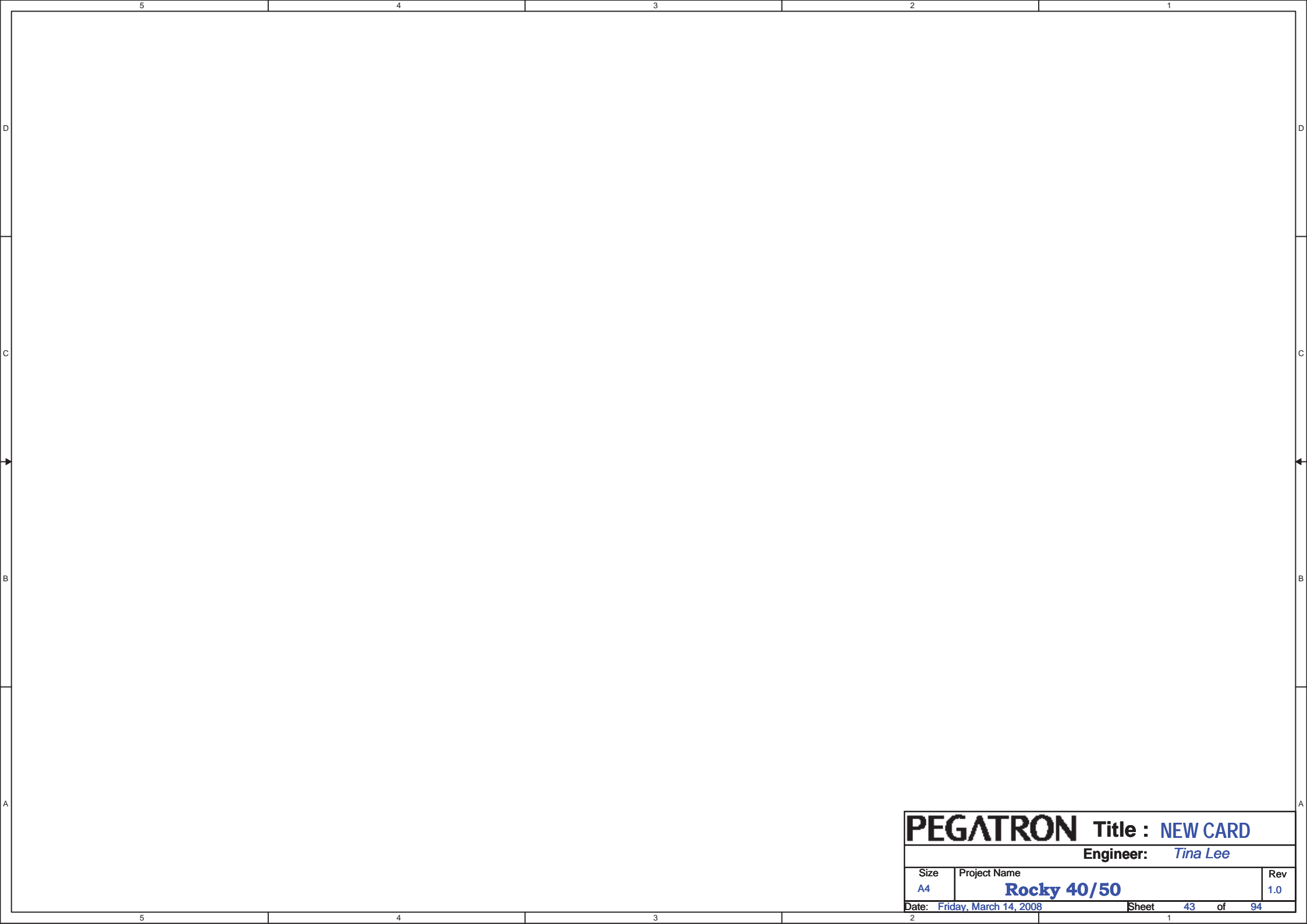




MDIO00--> SD Card Detect  
MDIO01--> MS Card Detect  
MDIO03--> SD Write Protect  
MDIO04--> SD Card Power0 Control/  
MS Power Control  
MDIO08--> SD Command/MS Bus State  
MDIO09--> SD Clock/MS Clock  
MDIO10--> SD Data 0/MS Data 0  
MDIO11--> SD Data 1/MS Data 1  
MDIO12--> SD Data 2/MS Data 2  
MDIO13--> SD Data 3/MS Data 3

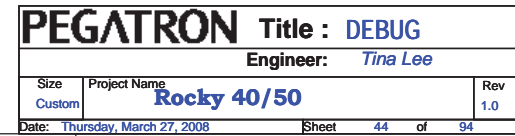
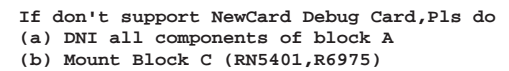
MDIO02--> xDCE#  
MDIO05--> SD Power Control 1 / xDWP  
MDIO06--> xD/MS/SD LED Control  
MDIO14--> xD Data  
MDIO15--> xD Data  
MDIO16--> xD Data  
MDIO17--> xD Data  
MDIO18--> xD CLE  
MDIO19--> xD ALE

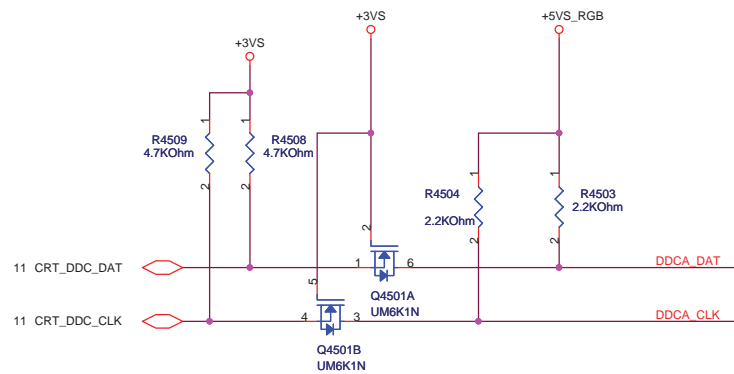
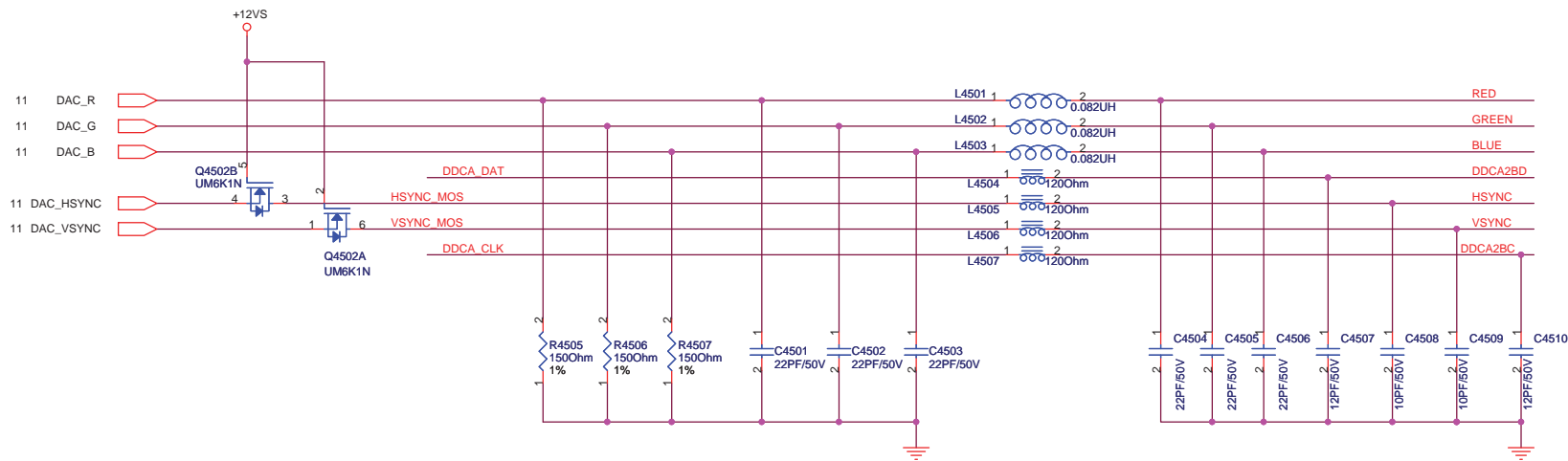




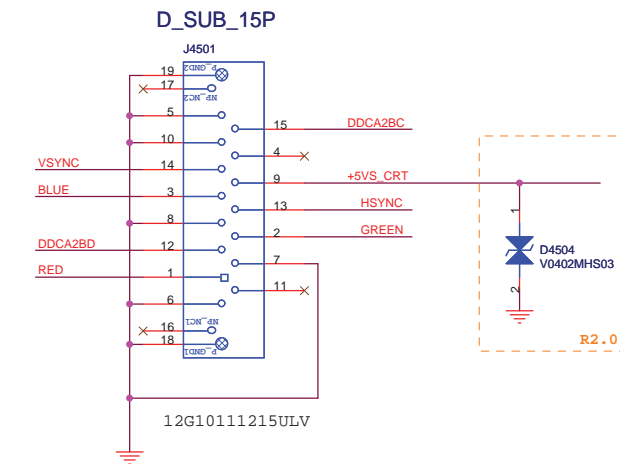
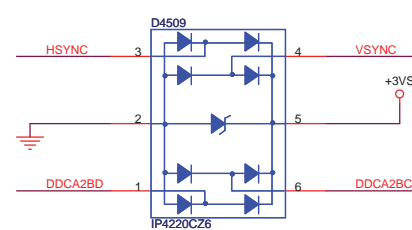
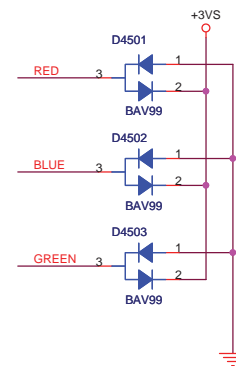
<b>PEGATRON</b>		<b>Title :</b> NEW CARD	
		<b>Engineer:</b> Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	43 of 94

## Block C

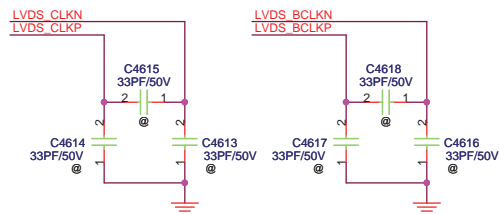
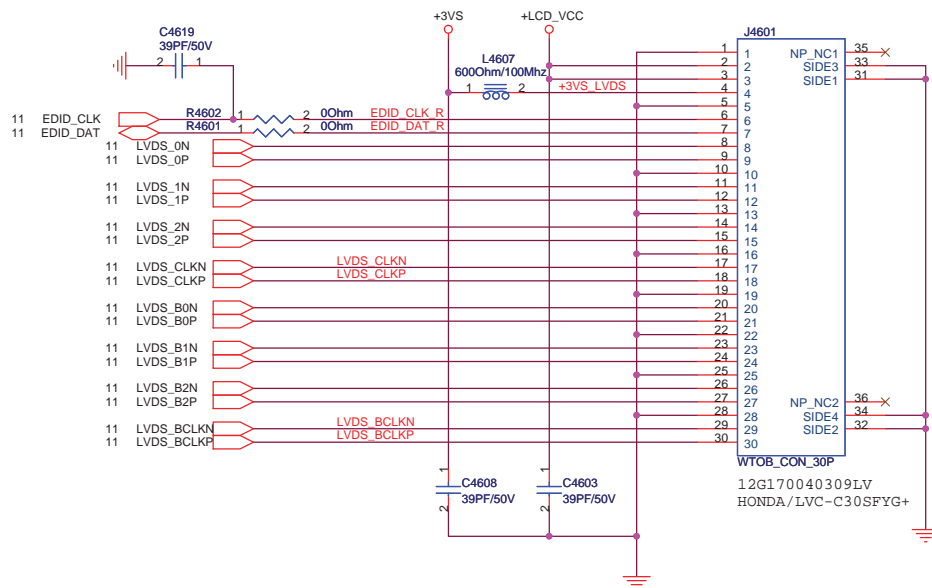




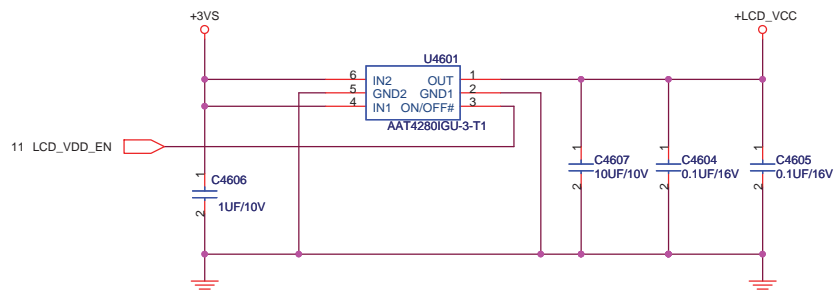
PLACE ESD Diodes near VGA port



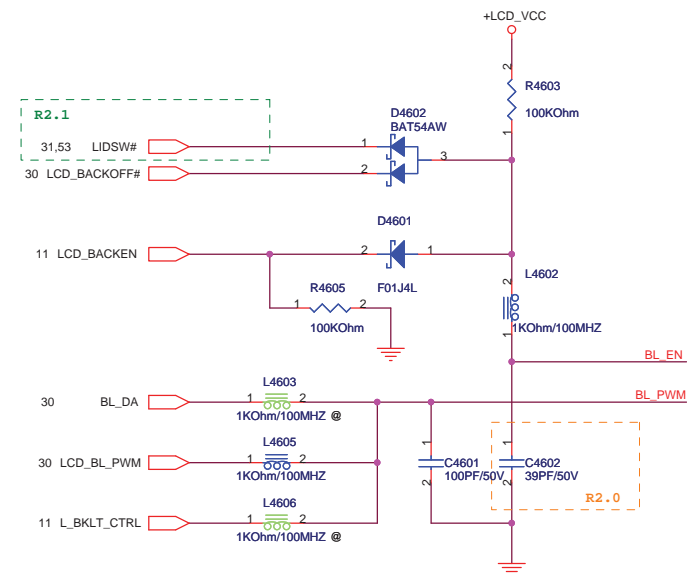
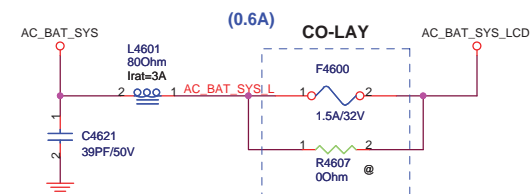
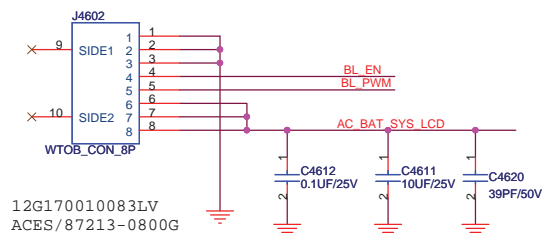
## LVDS CNT

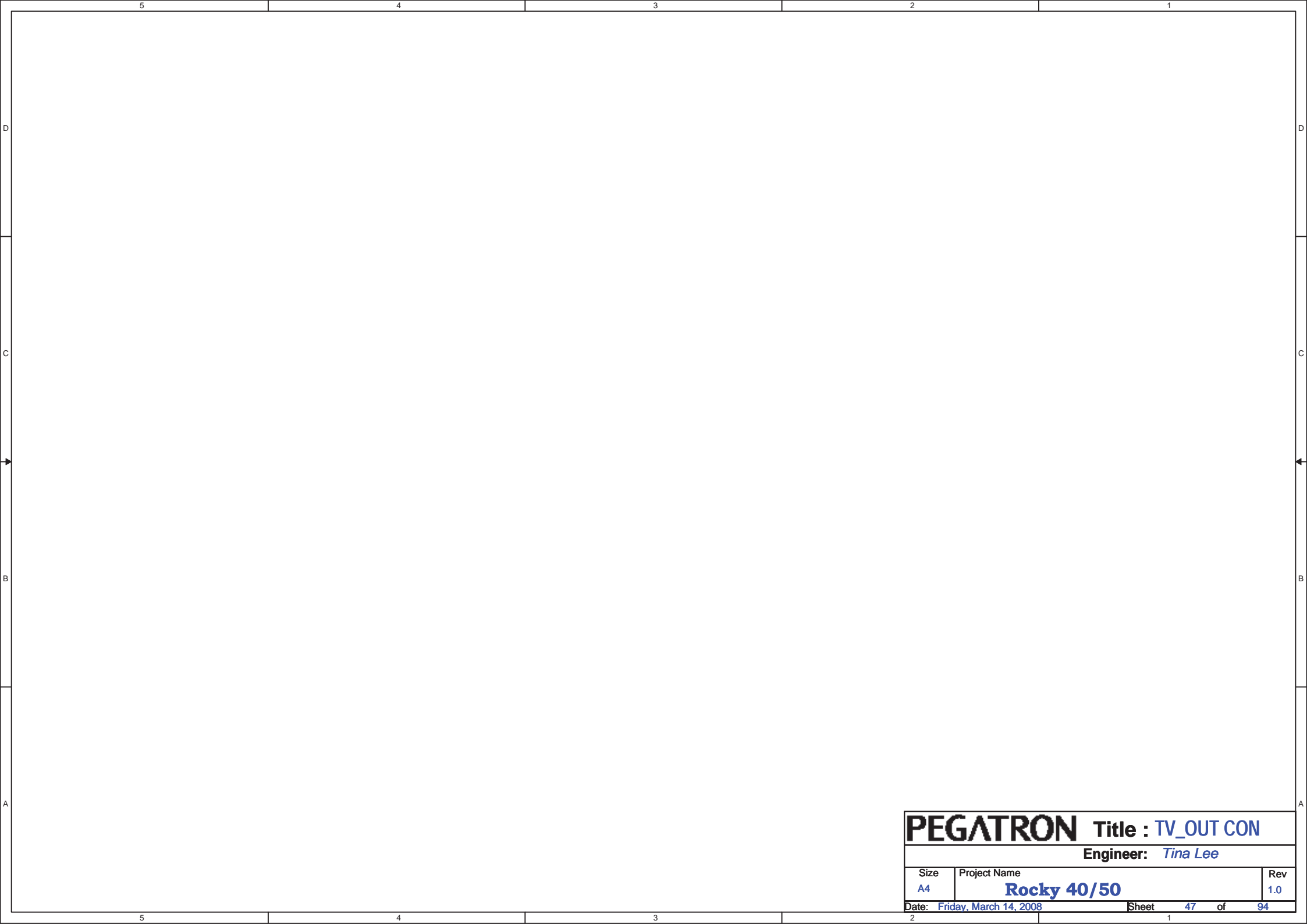


## Power Switch for LCD Power



## INVERTOR CNT



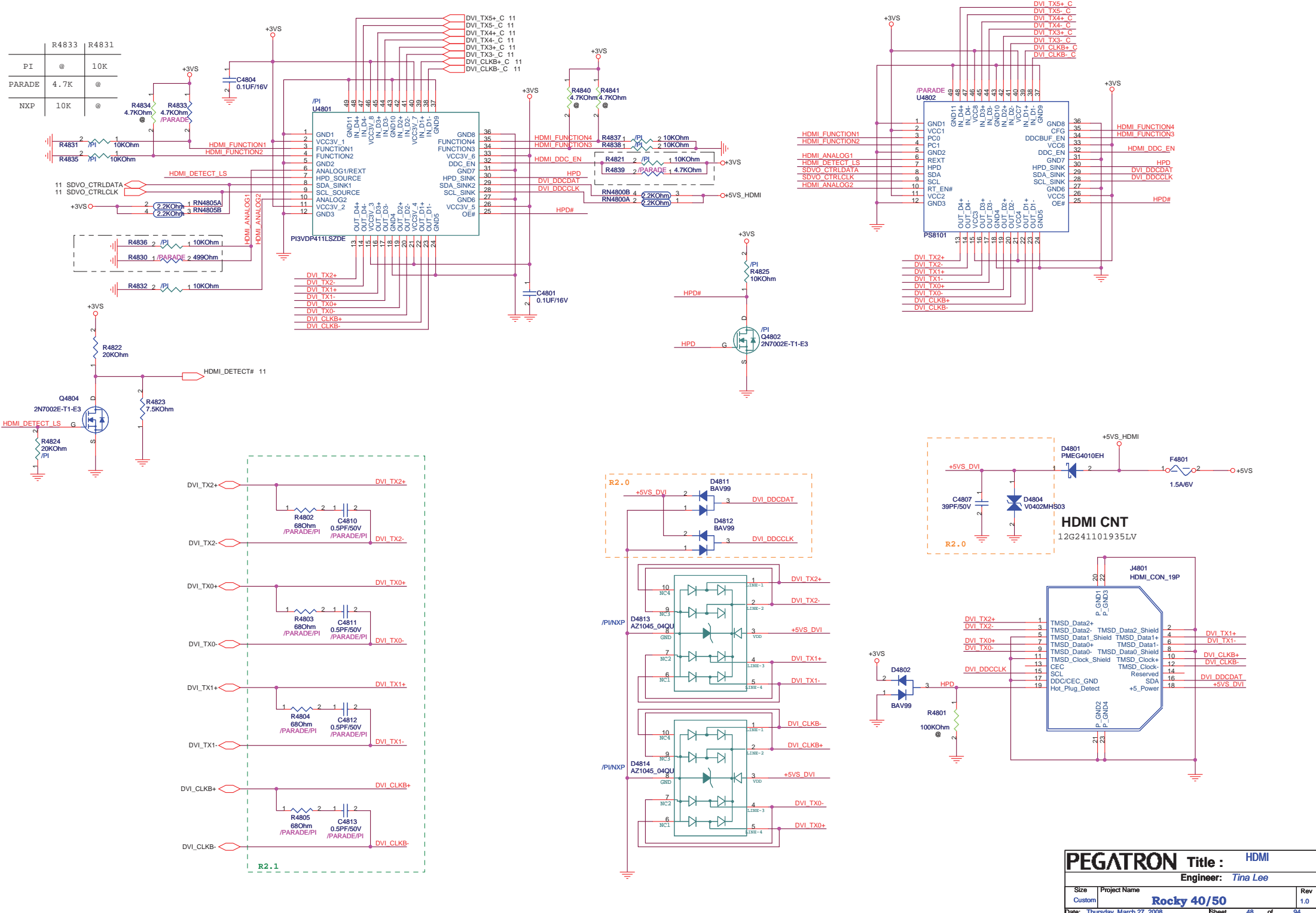


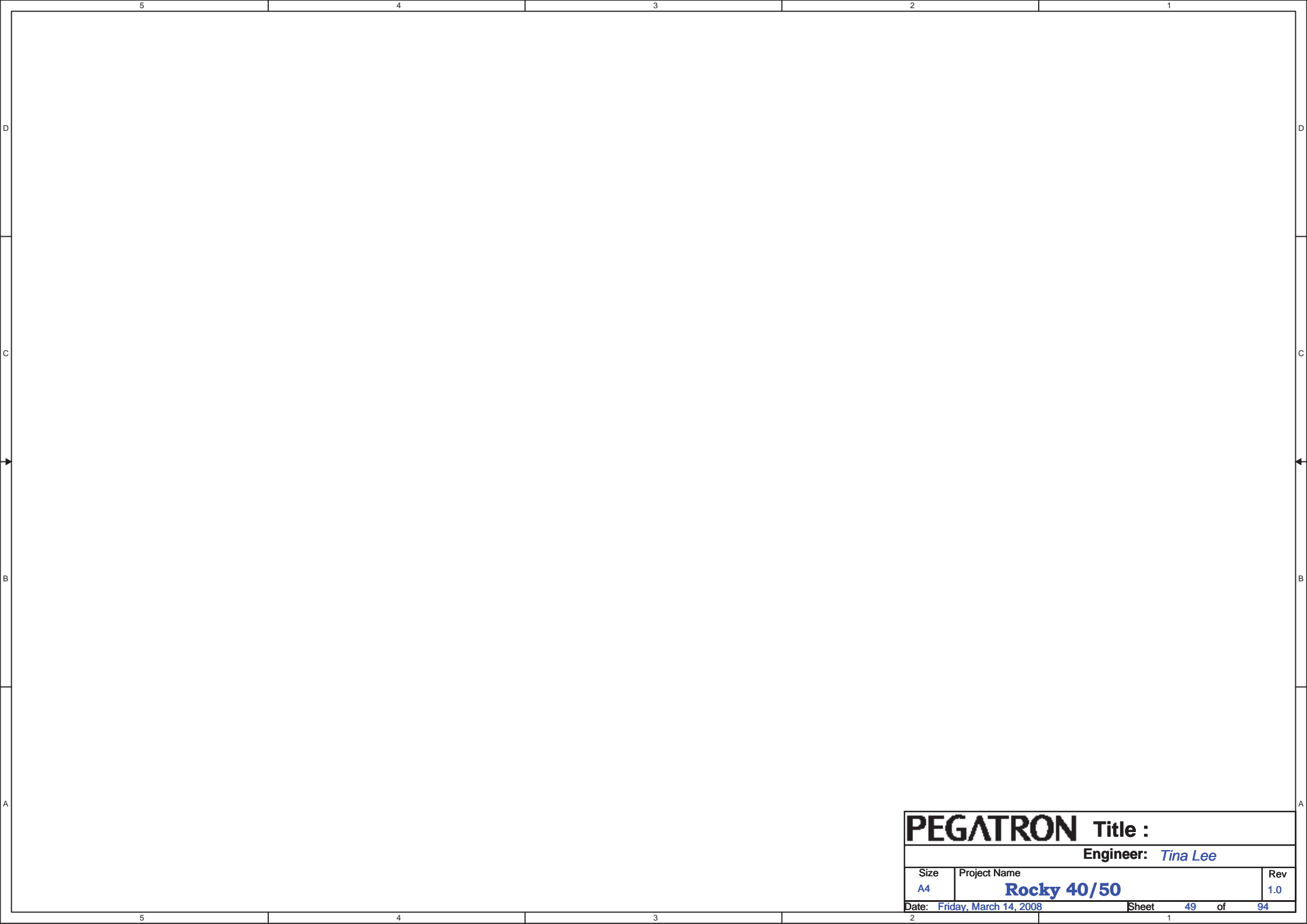
PEGATRON

Title : TV\_OUT CON

Engineer: Tina Lee

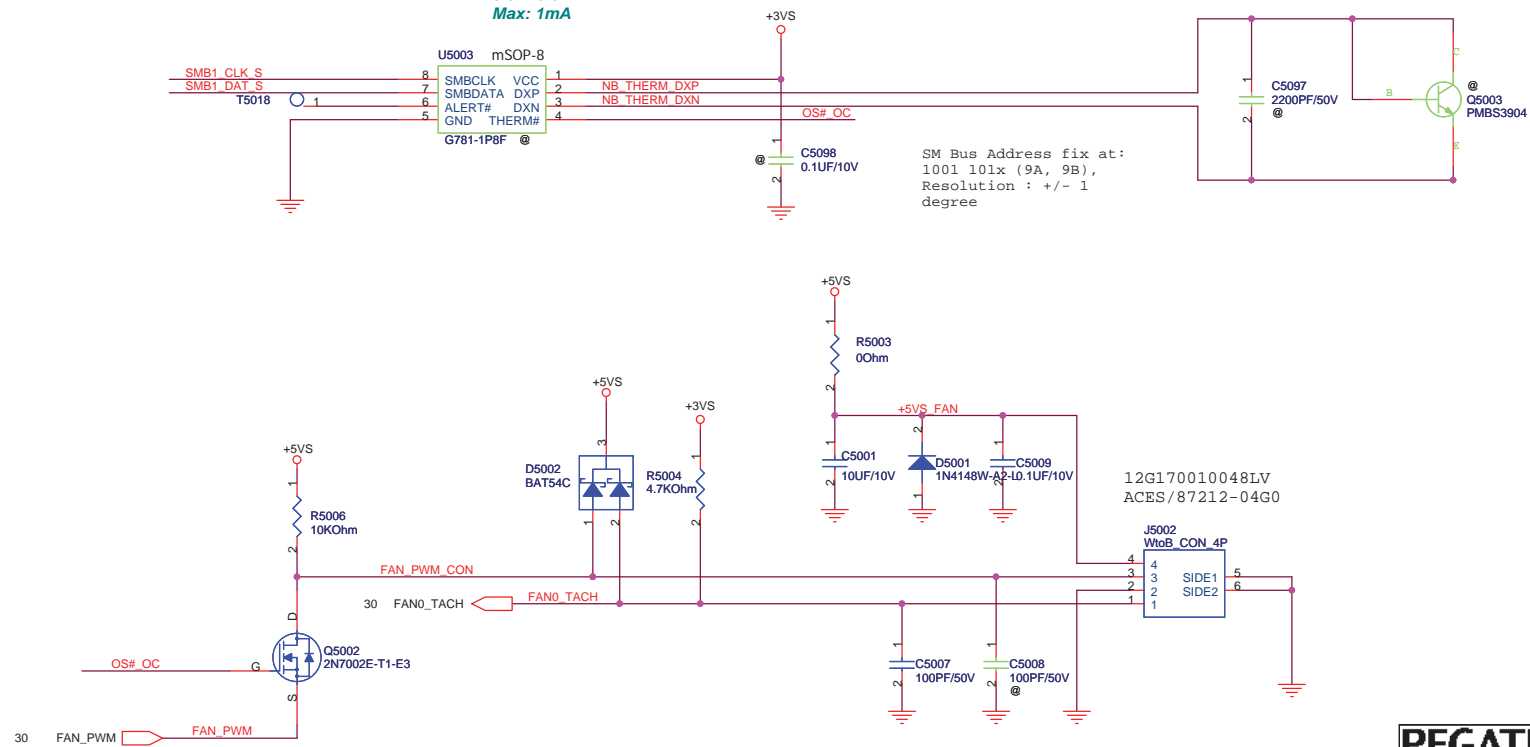
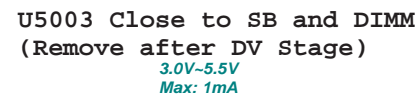
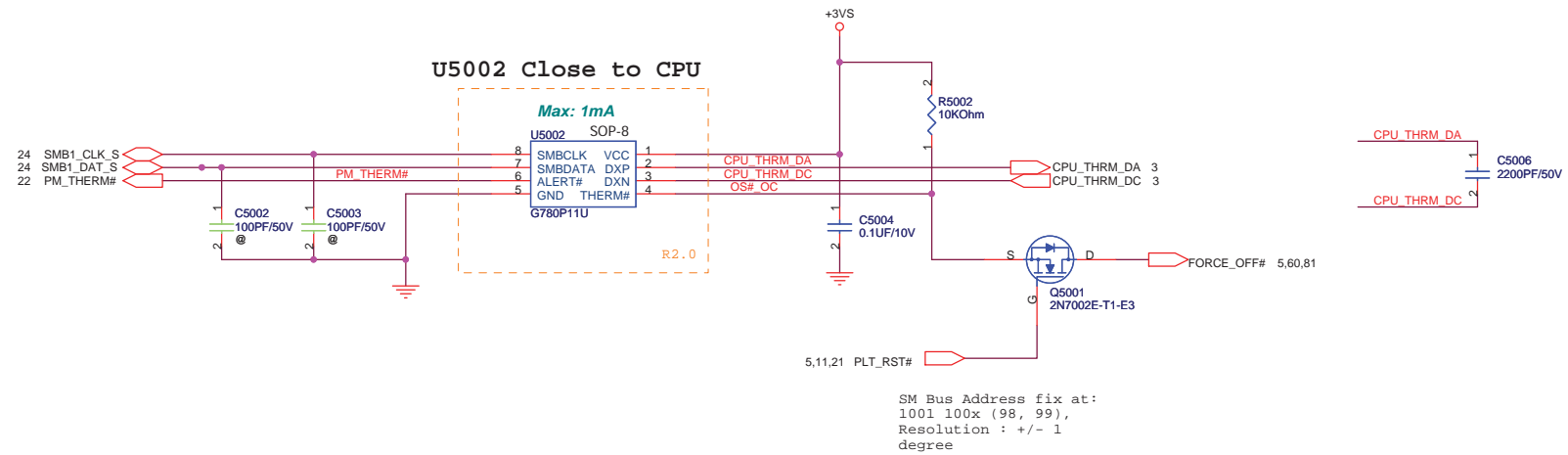
Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 47 of 94	



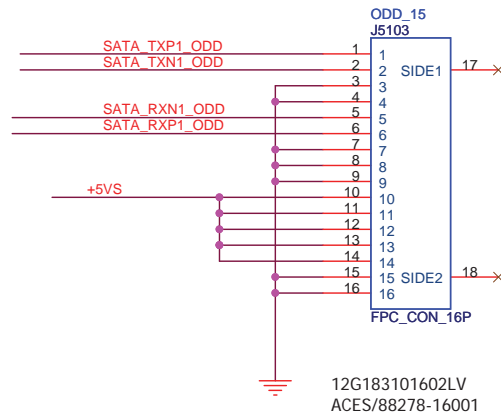
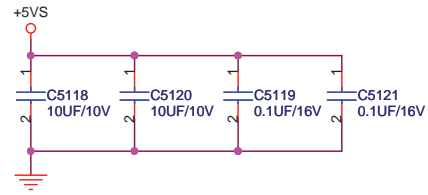
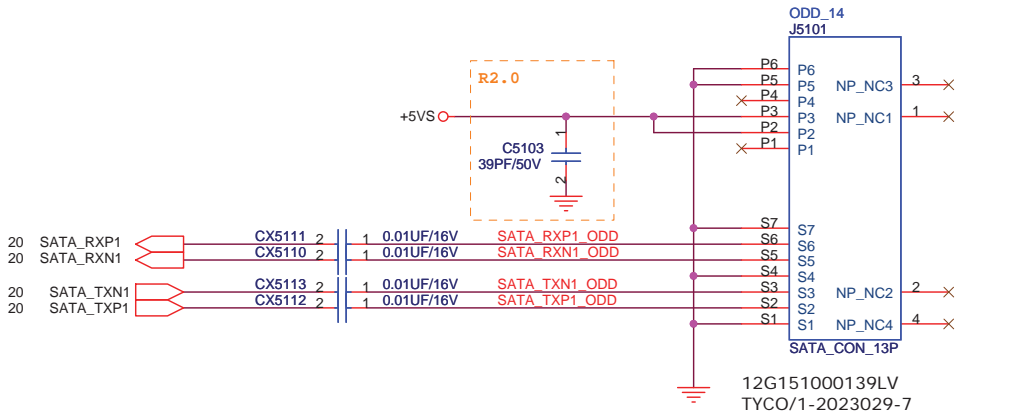


PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	49	of 94

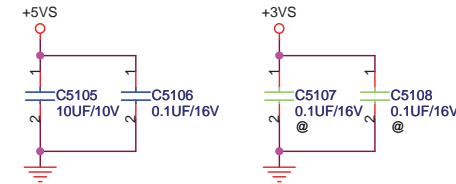
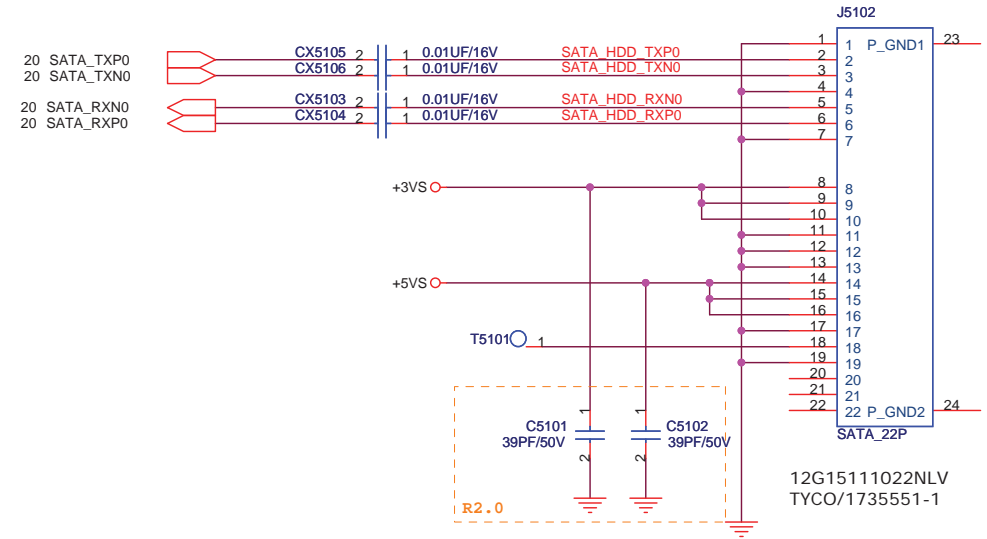
## Thermal Sensor

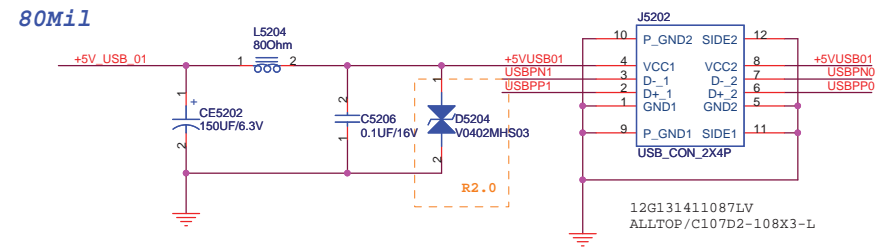
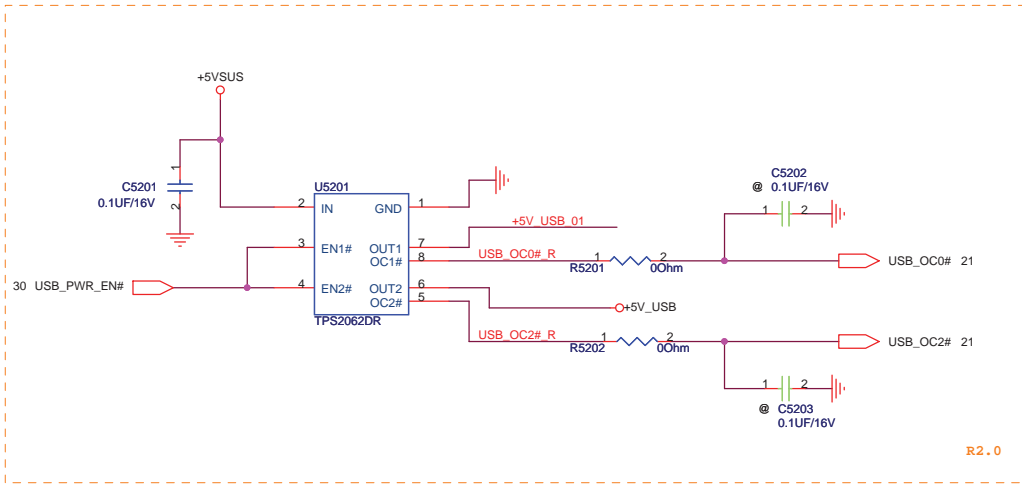
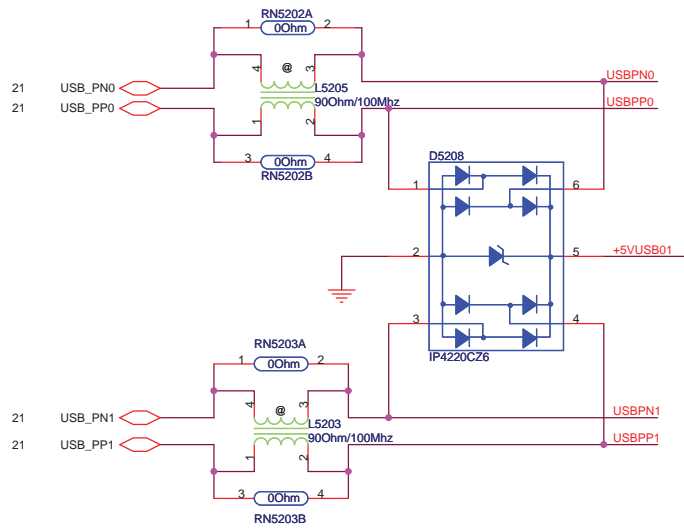


## ODD CON

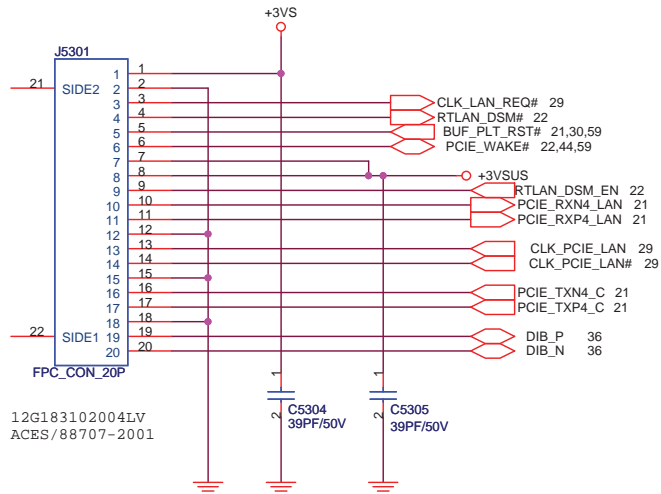


## SATA HDD CON

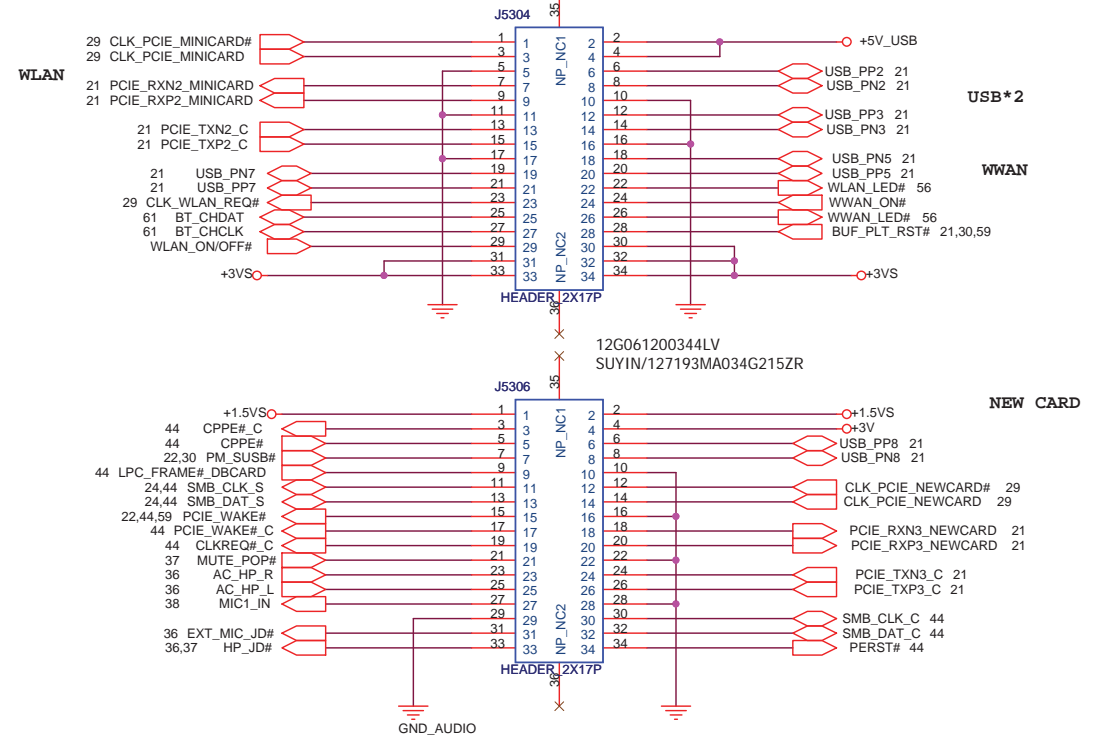




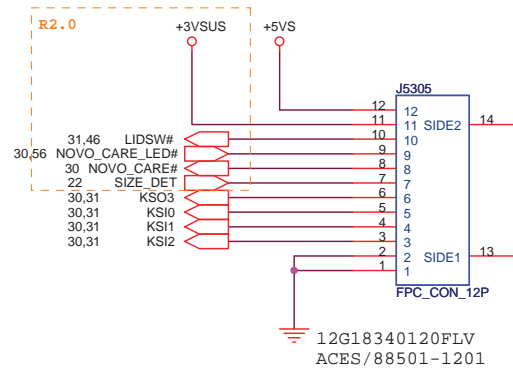
## IO BOARD



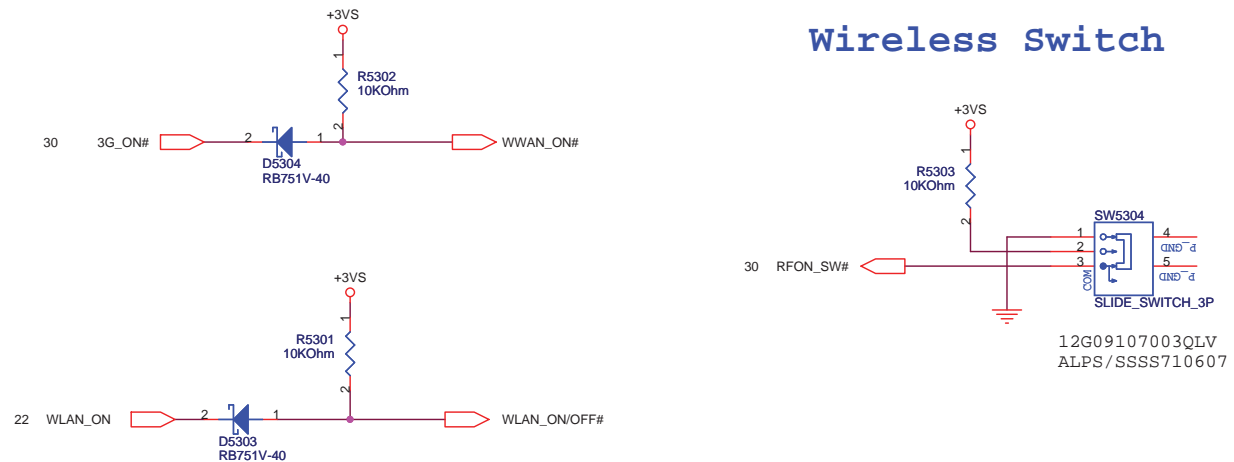
## SMALL BOARD

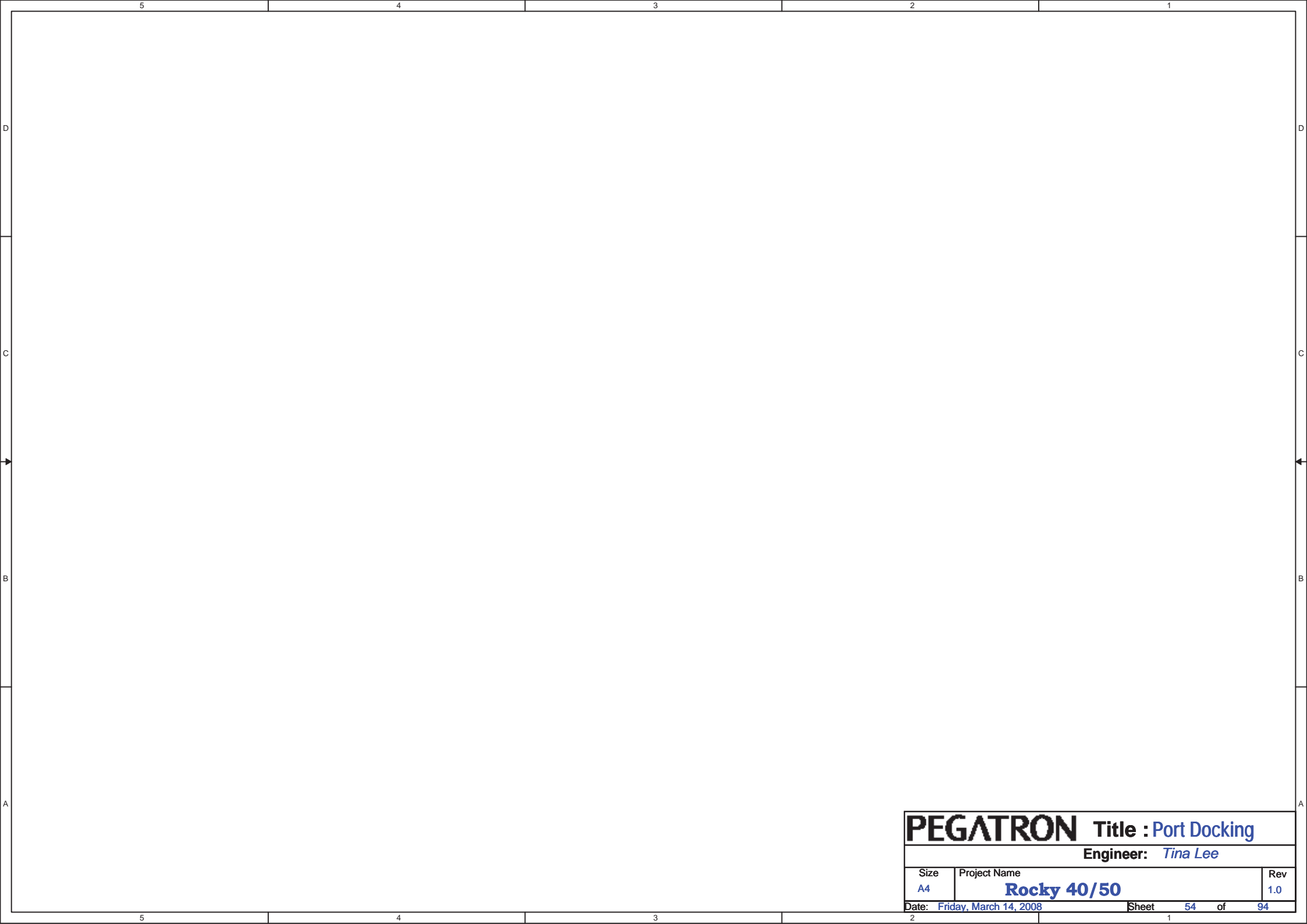


## For Media Control Board



## Wireless Switch



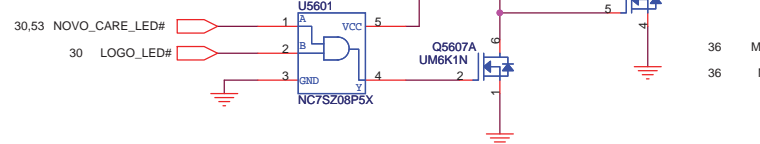
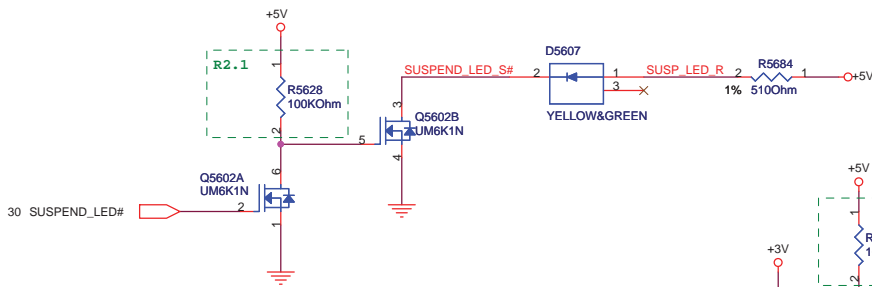
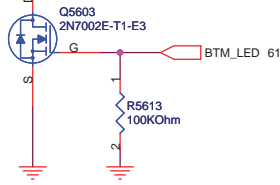
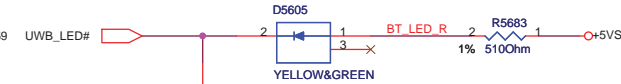
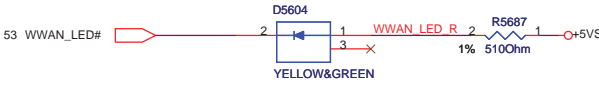
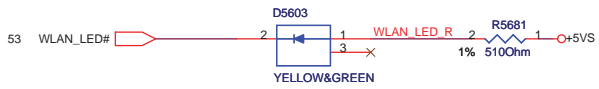
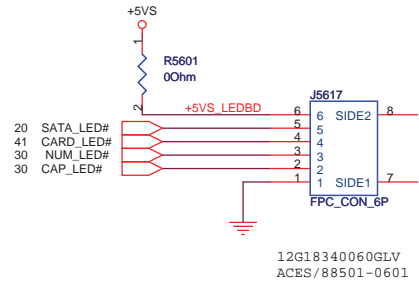


<b>PEGATRON</b>		<b>Title :</b> <b>Port Docking</b>	
<b>Engineer:</b> <i>Tina Lee</i>			
Size	Project Name		Rev
A4	<b>Rocky 40/50</b>		1.0
Date: <b>Friday, March 14, 2008</b>		Sheet	<b>54</b> of <b>94</b>

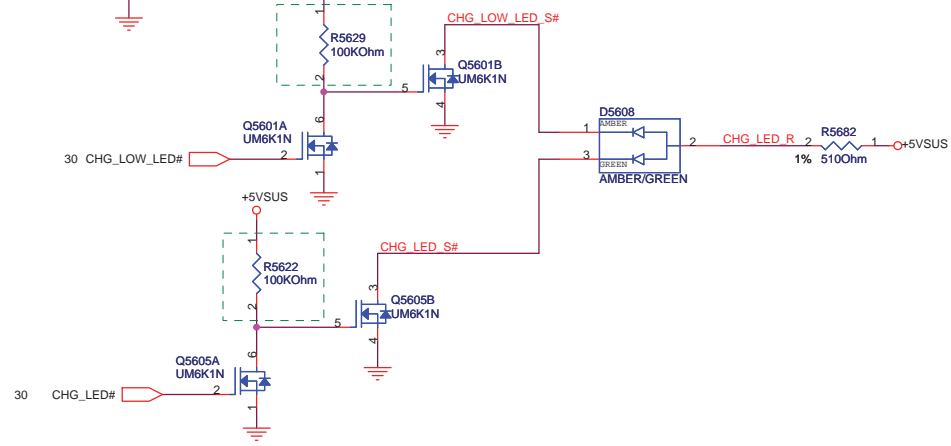
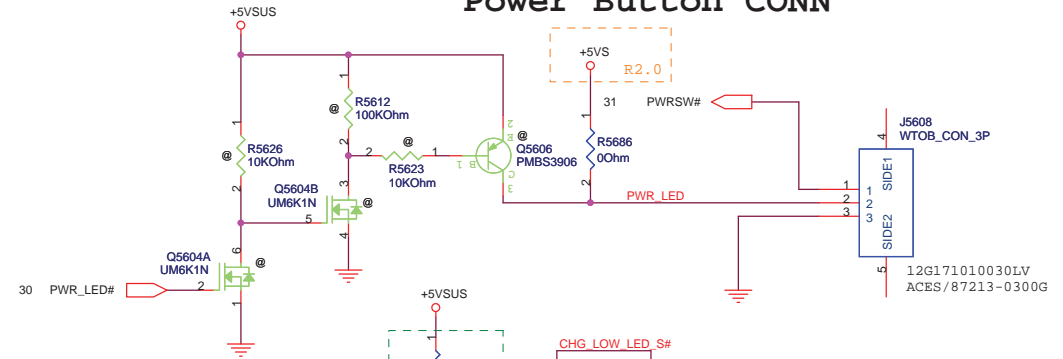
	A	B	C	D	E
1					
2					
3					
4					
5					

<b>PEGATRON</b>			Title : <i>Super I/O &amp; FIR</i>		
			Engineer: <i>Tina Lee</i>		
Size	Project Name				Rev
<i>A4</i>	<b>Rocky 40/50</b>				1.0
Date: <i>Friday, March 14, 2008</i>			Sheet	<i>55</i>	of <i>94</i>

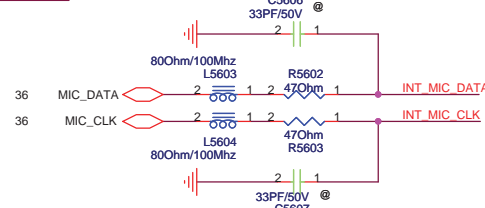
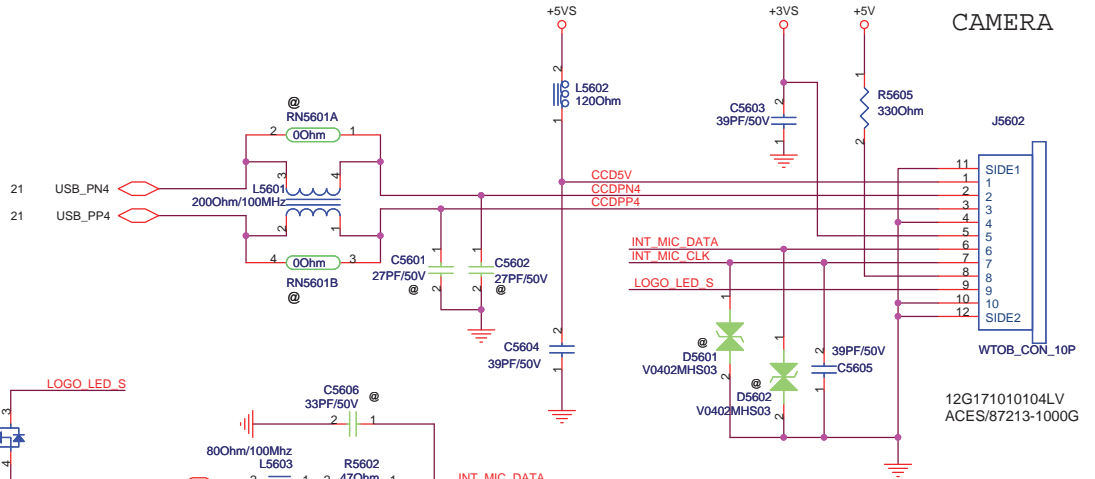
## LED CONN



## Power Button CONN

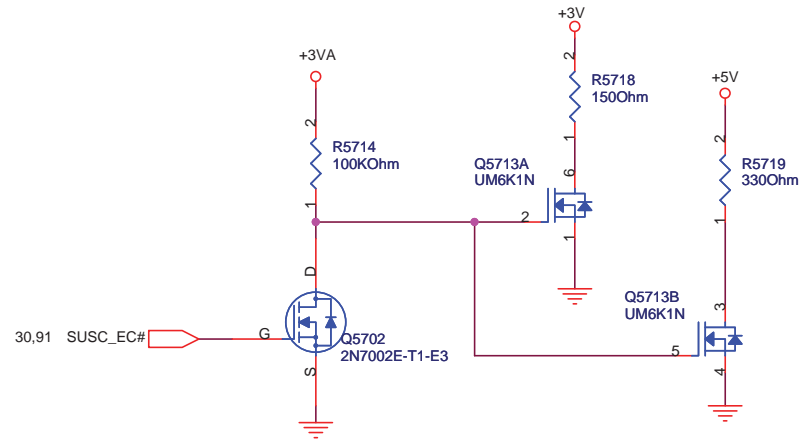
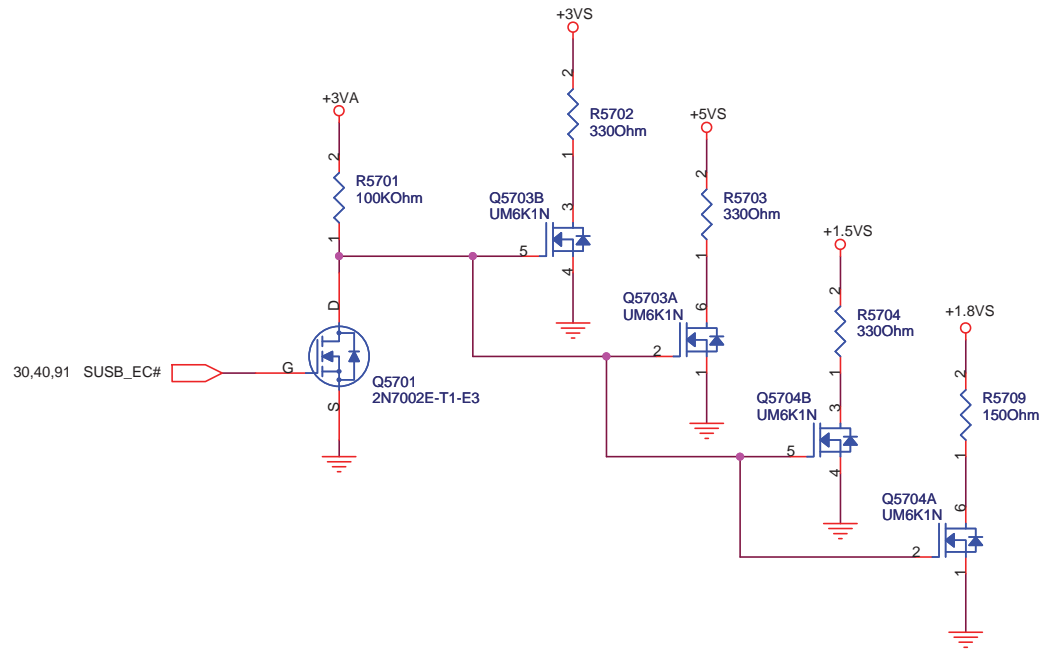


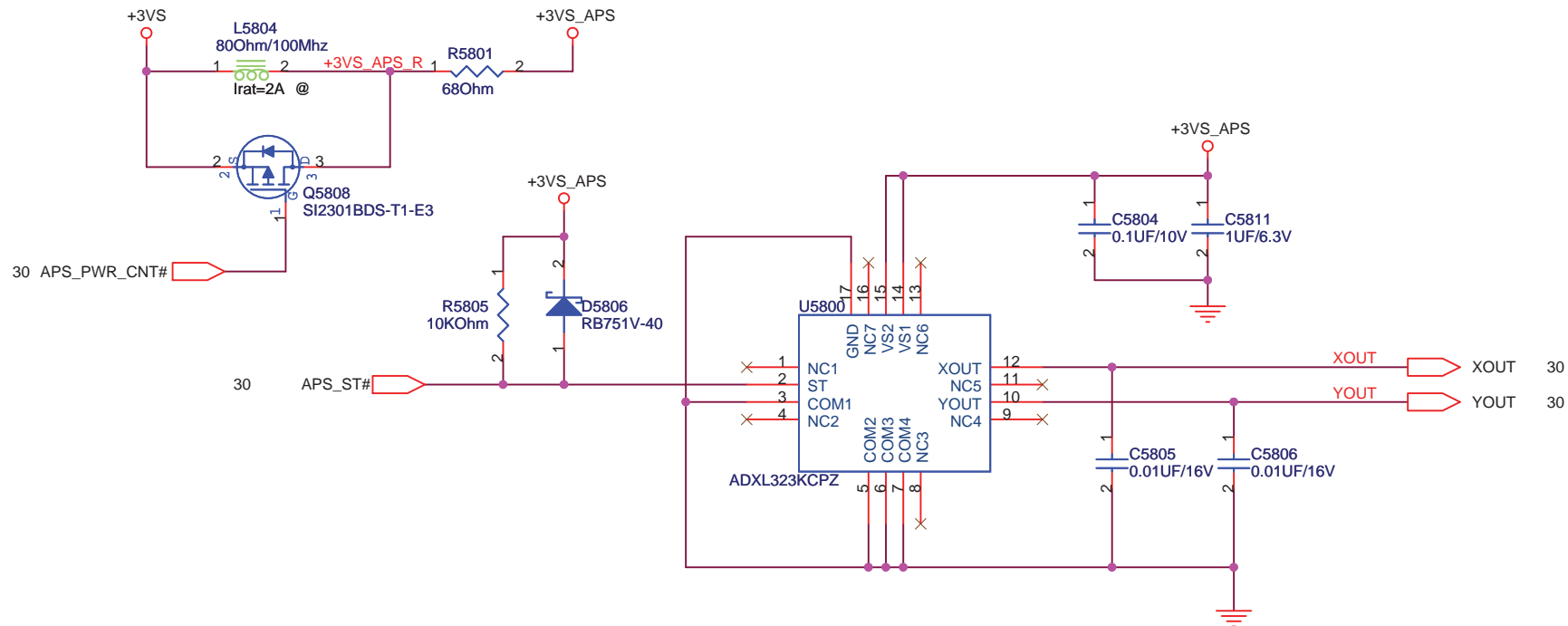
## CAMERA



**PEGATRON** Title : LED/TP/SW  
Engineer: Tina Lee

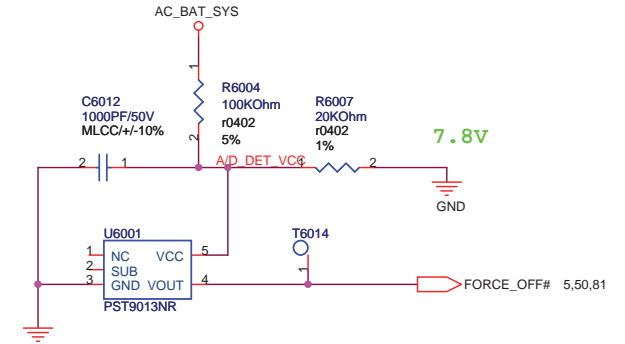
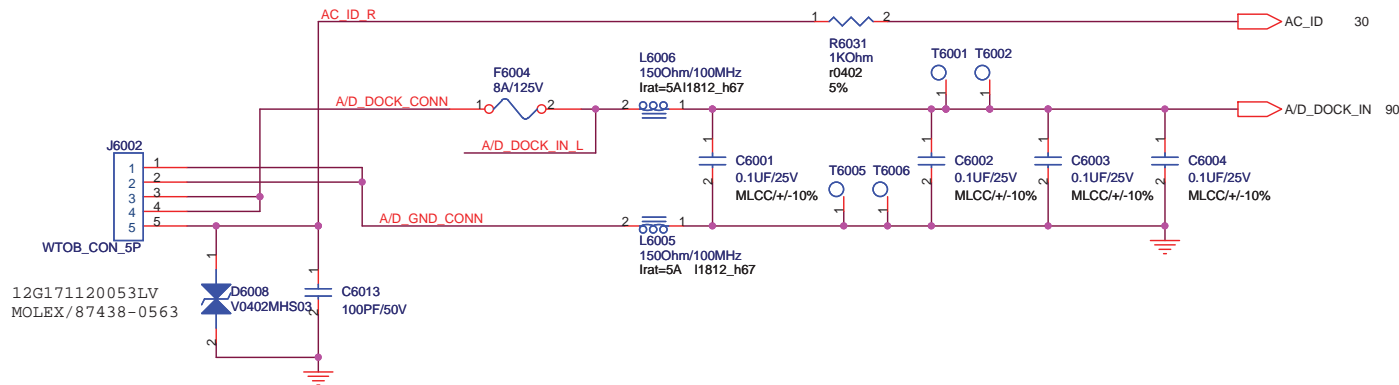
Size	Project Name	Rev
Custom	Rocky 40/50	1.0
Date: Thursday, March 27, 2008	Sheet 56 of 94	





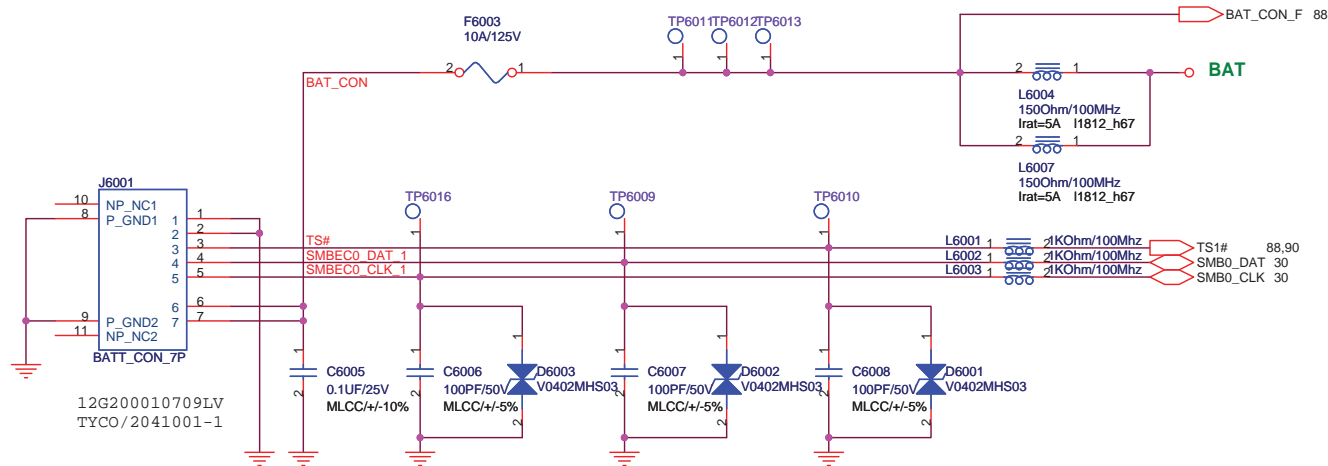


## DC IN CONN



Without Battery & Pull out Adapter

## Battery CONN

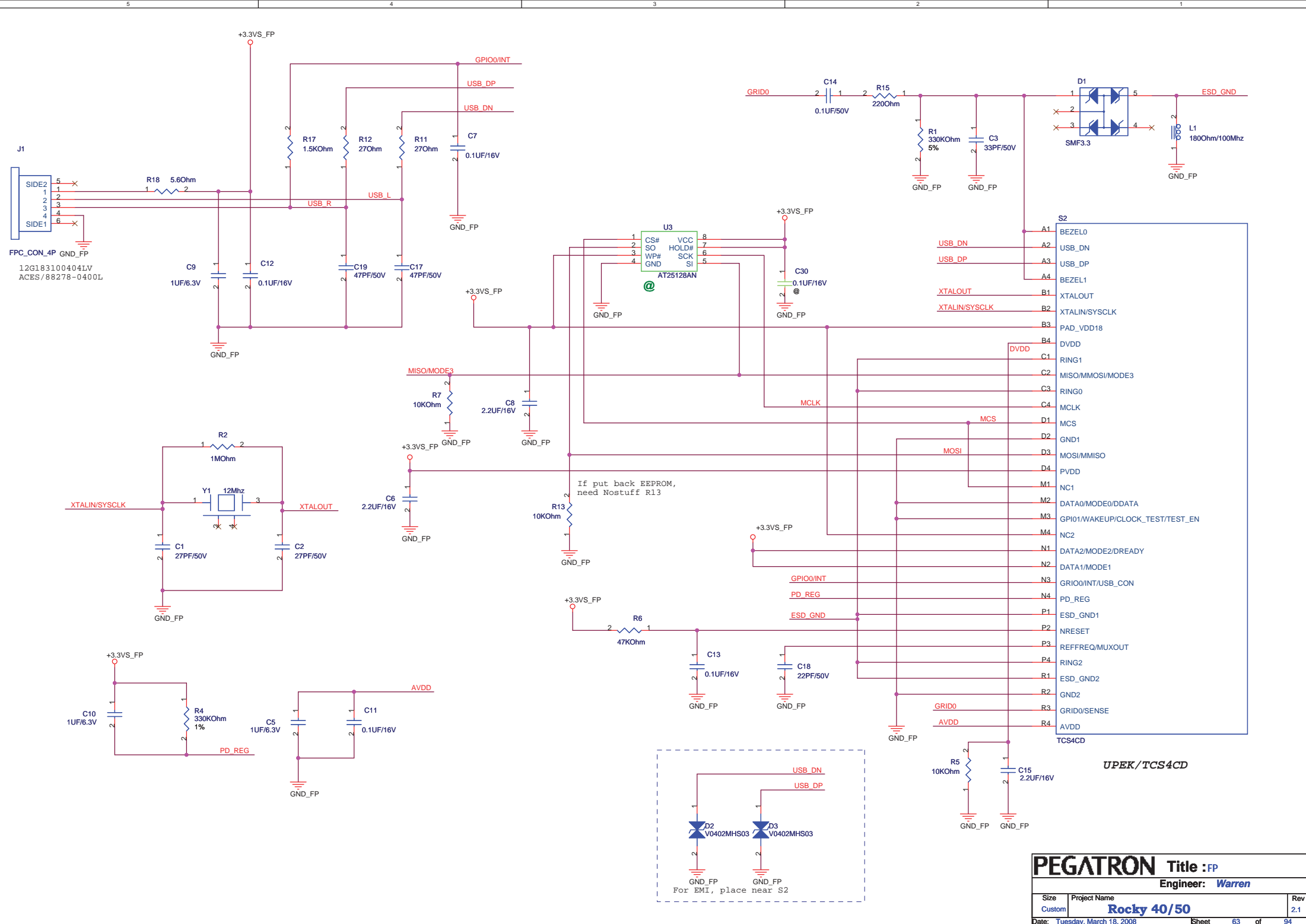


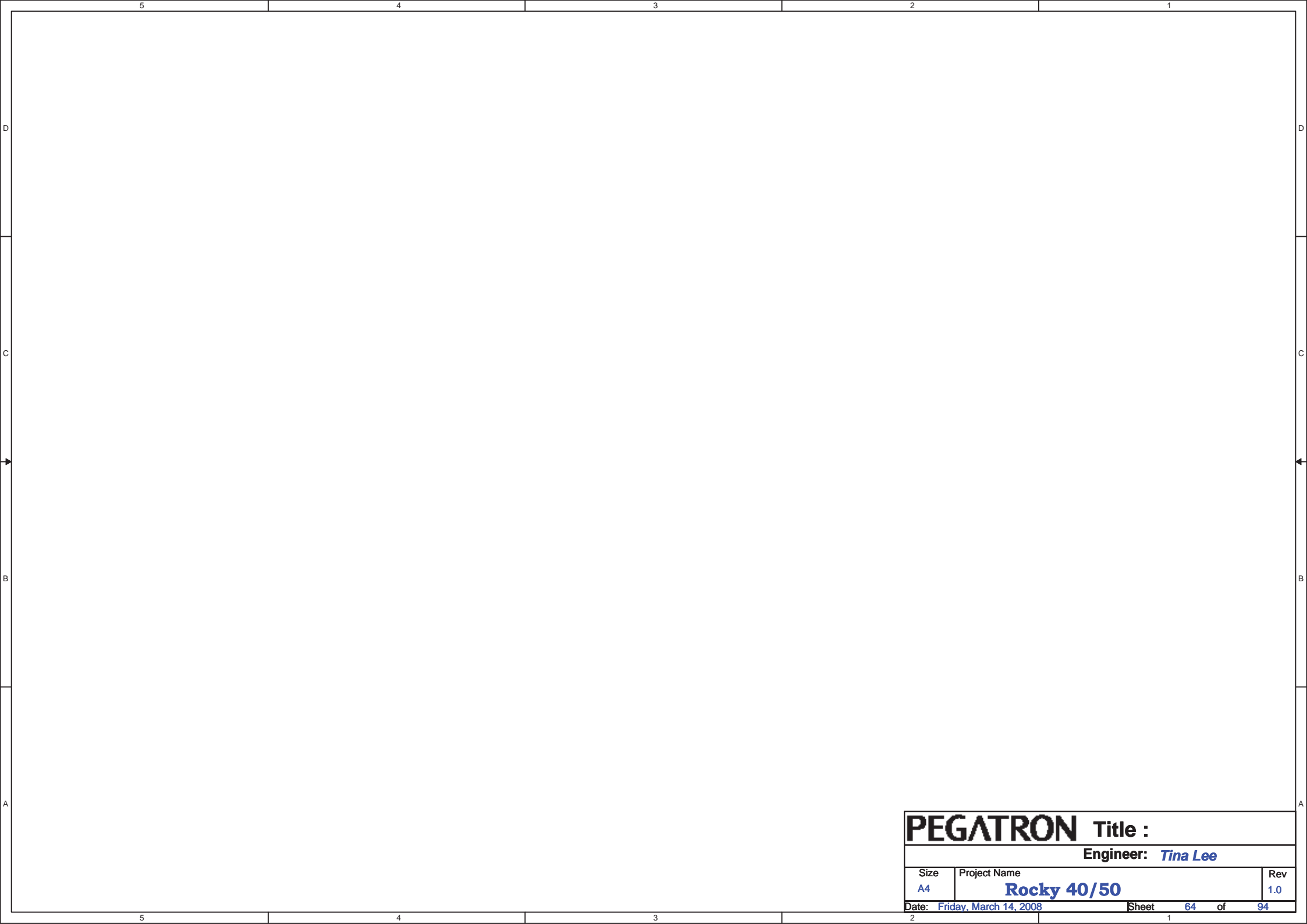
## 1



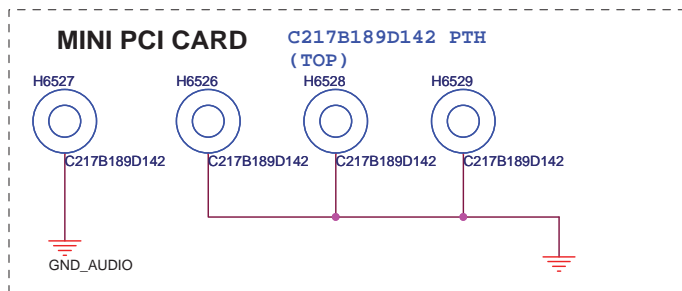
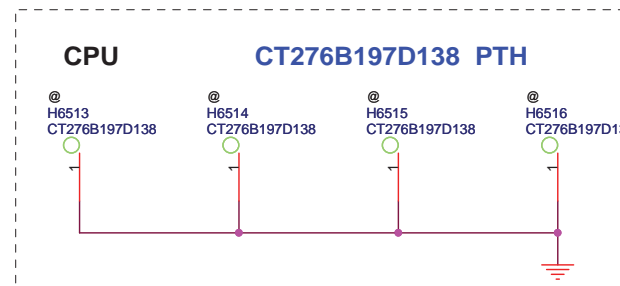
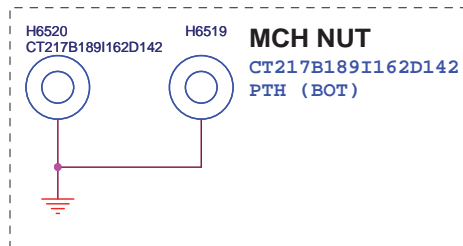
5	4	3	2	1
D				D
C				C
B				B
A				A

PEGATRON			Title : <i>TPM</i>		
Engineer: <i>Tina Lee</i>					
Size	Project Name				Rev
<i>A4</i>	<b>Rocky 40/50</b>				<i>1.0</i>
Date: <i>Friday, March 14, 2008</i>			Sheet	<i>62</i>	of <i>94</i>

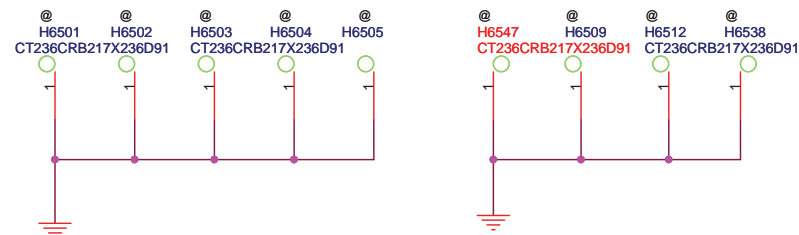




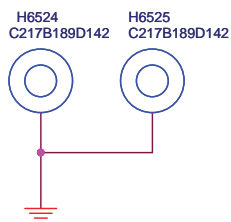
PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	64	of 94



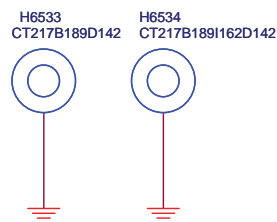
### MLB BOT - TOP SCREW HOLE CT236CRB217X236D91 PTH



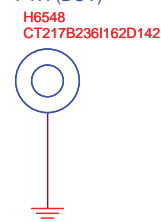
For Fan Stand Off  
 C217B189D142 PTH (mirror/BOT)



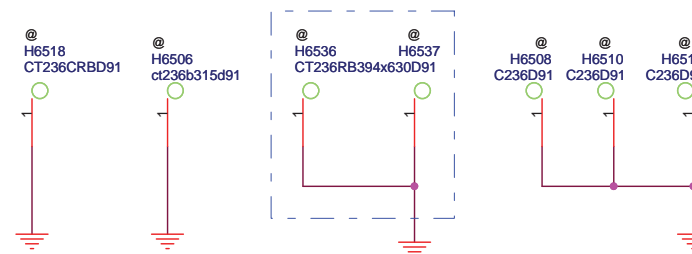
For KB Stand Off  
 CT217B189D142 PTH (TOP)



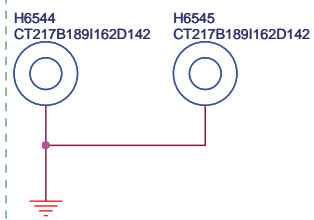
For MLB Stand Off  
 CT217B236I162D142 PTH (BOT)



### MLB SCREW HOLE PTH



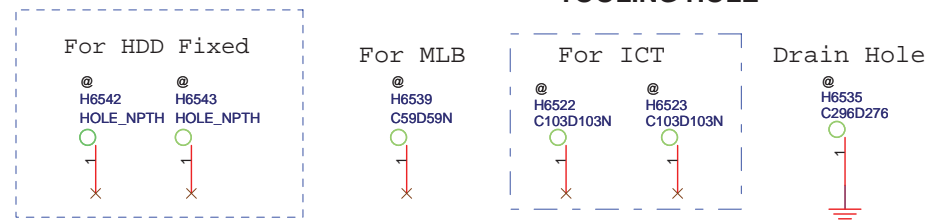
For HDD StandOff  
 (BOT)



For BT StandOff  
 (TOP) 5.5 PAD

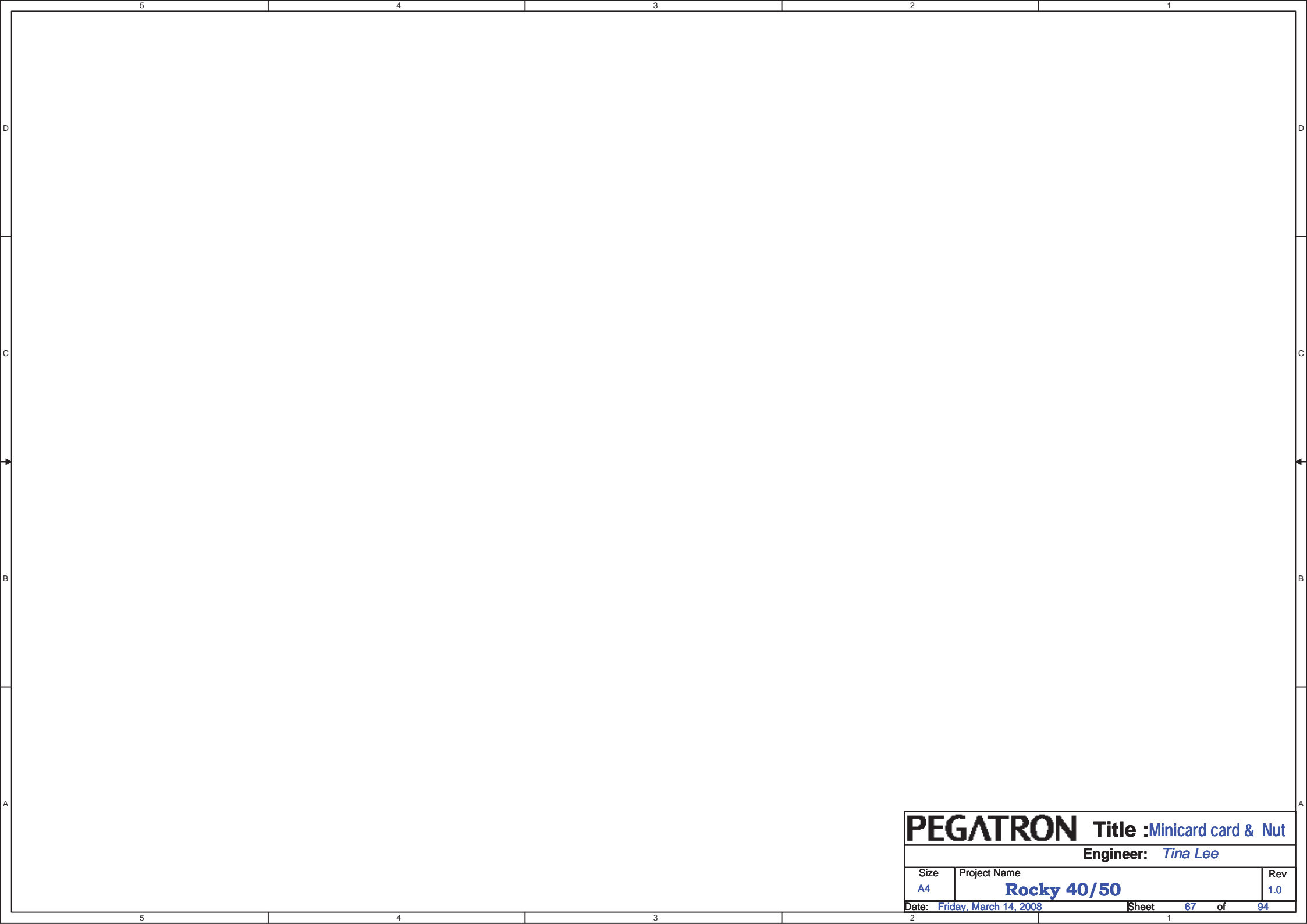


### TOOLING HOLE



A	B	C	D	E
E				
D				
C				
B				
A				

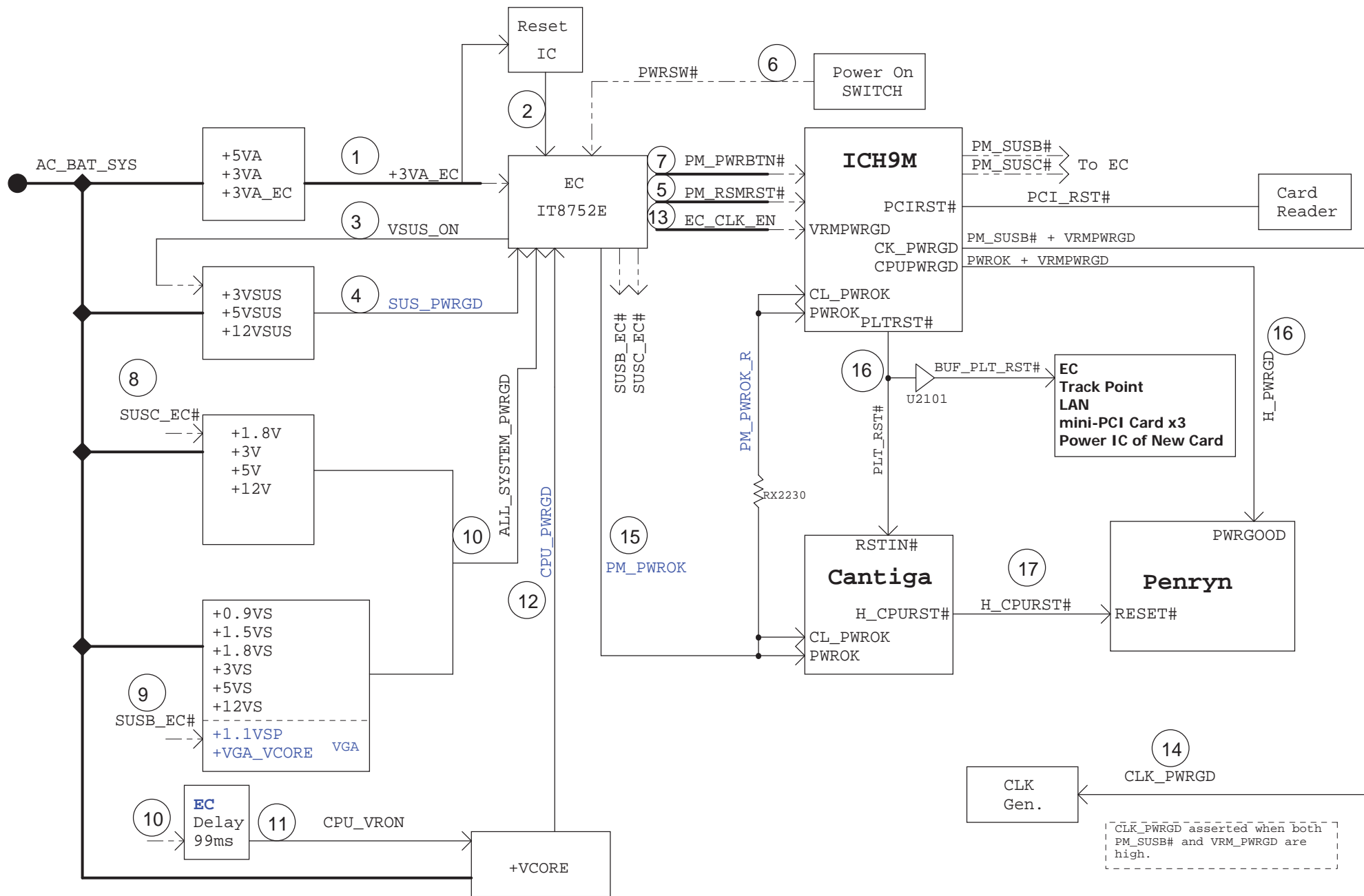
<b>PEGATRON</b>		<b>Title :</b> E-SATA	
<b>Engineer:</b> Tina Lee			
Size A4	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Friday, March 14, 2008		Sheet 66	of 94



<b>PEGATRON</b>		<b>Title :</b> Minicard card & Nut	
<b>Engineer:</b> Tina Lee			
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	67 of 94

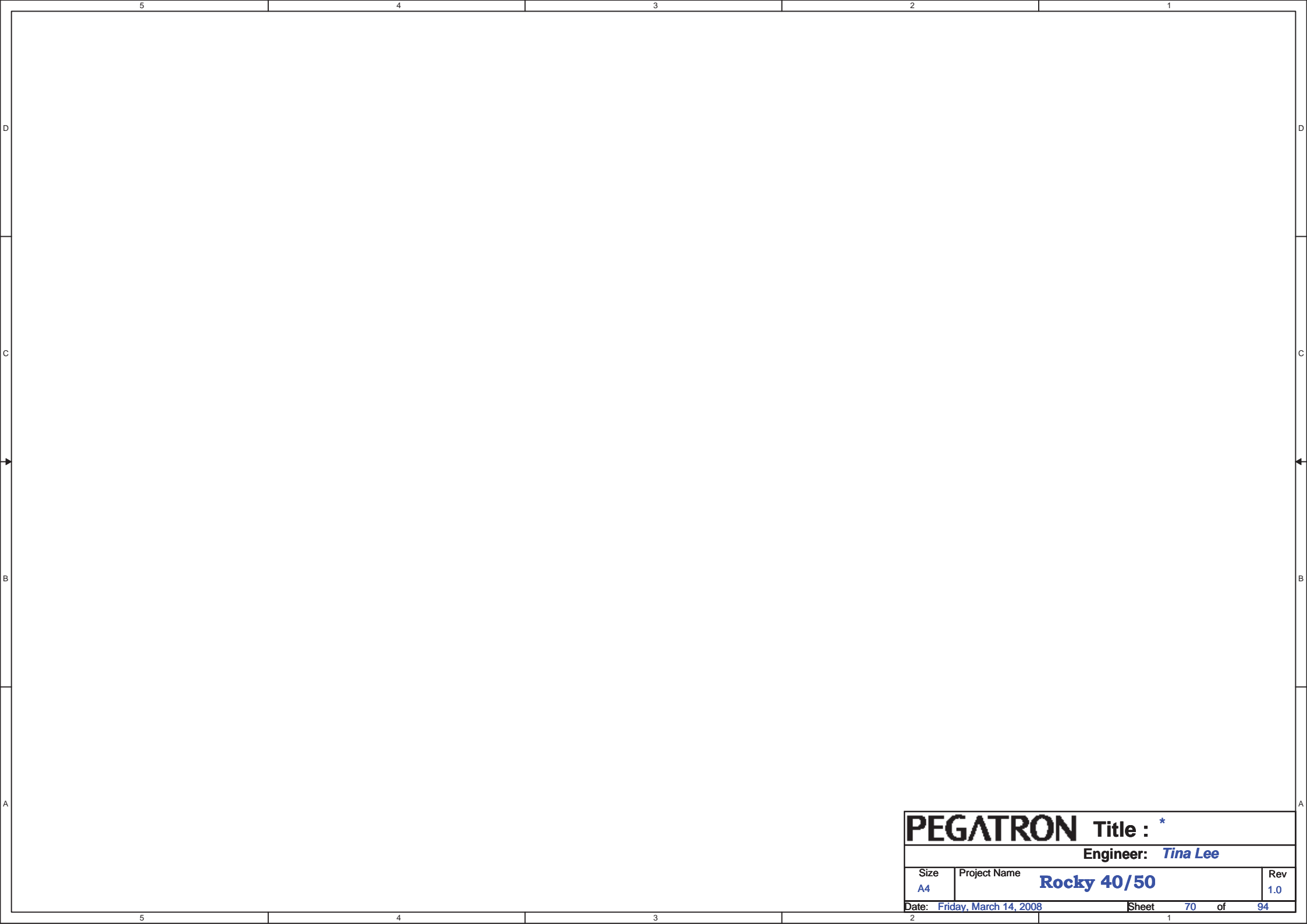
5	4	3	2	1
D				
C				
B				
A				

<b>PEGATRON</b>			Title : <b>XDP</b>		
			Engineer: <i>Tina Lee</i>		
Size	Project Name				Rev
A4	<b>Rocky 40/50</b>				1.0
Date: <u>Friday, March 14, 2008</u>			Sheet	68	of 94



## Power On Sequence

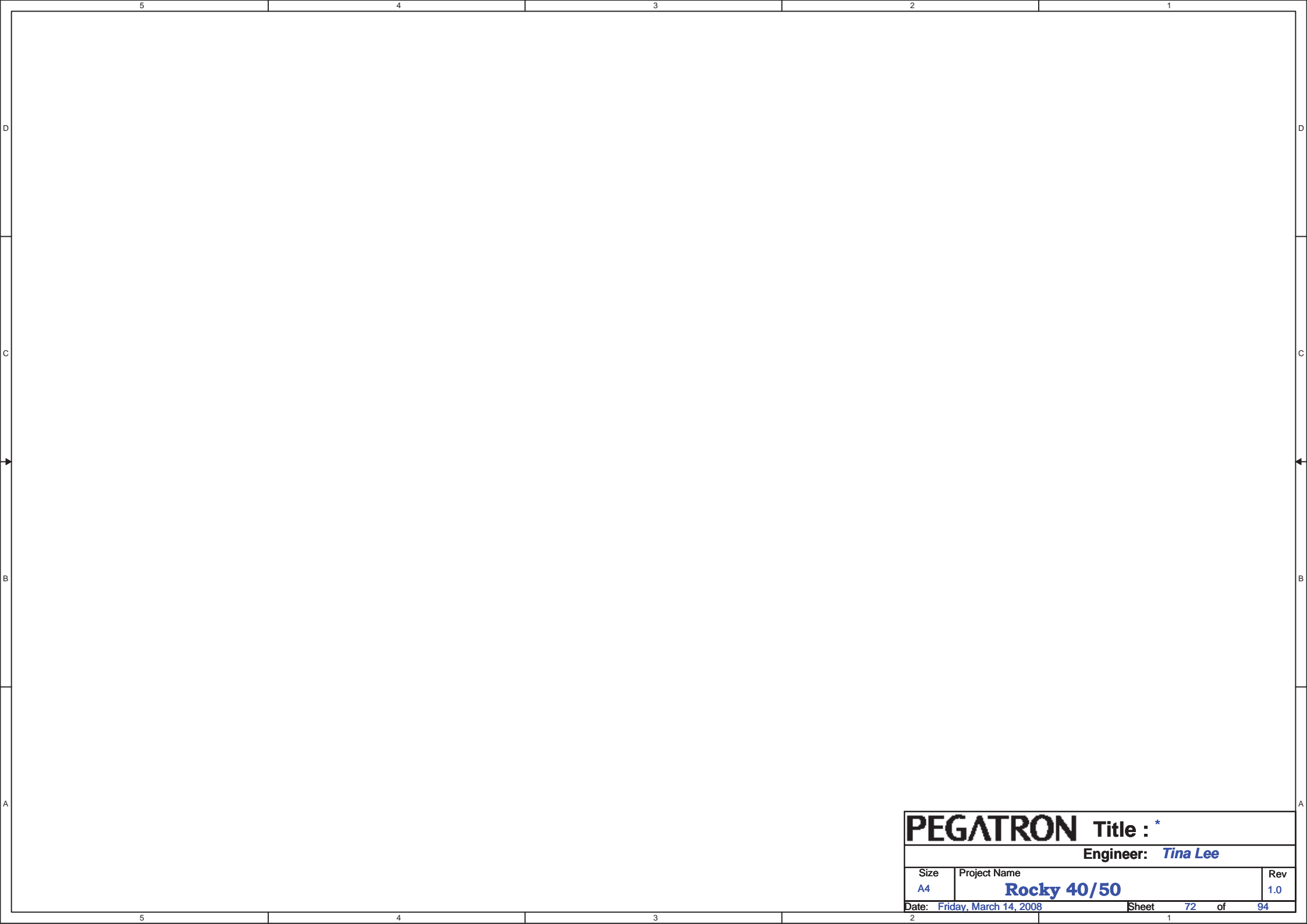




PEGATRON			Title : *		
			Engineer: Tina Lee		
Size	Project Name			Rev	
A4	Rocky 40/50			1.0	
Date: Friday, March 14, 2008			Sheet	70	of 94

5	4	3	2	1
D				
C				
B				
A				

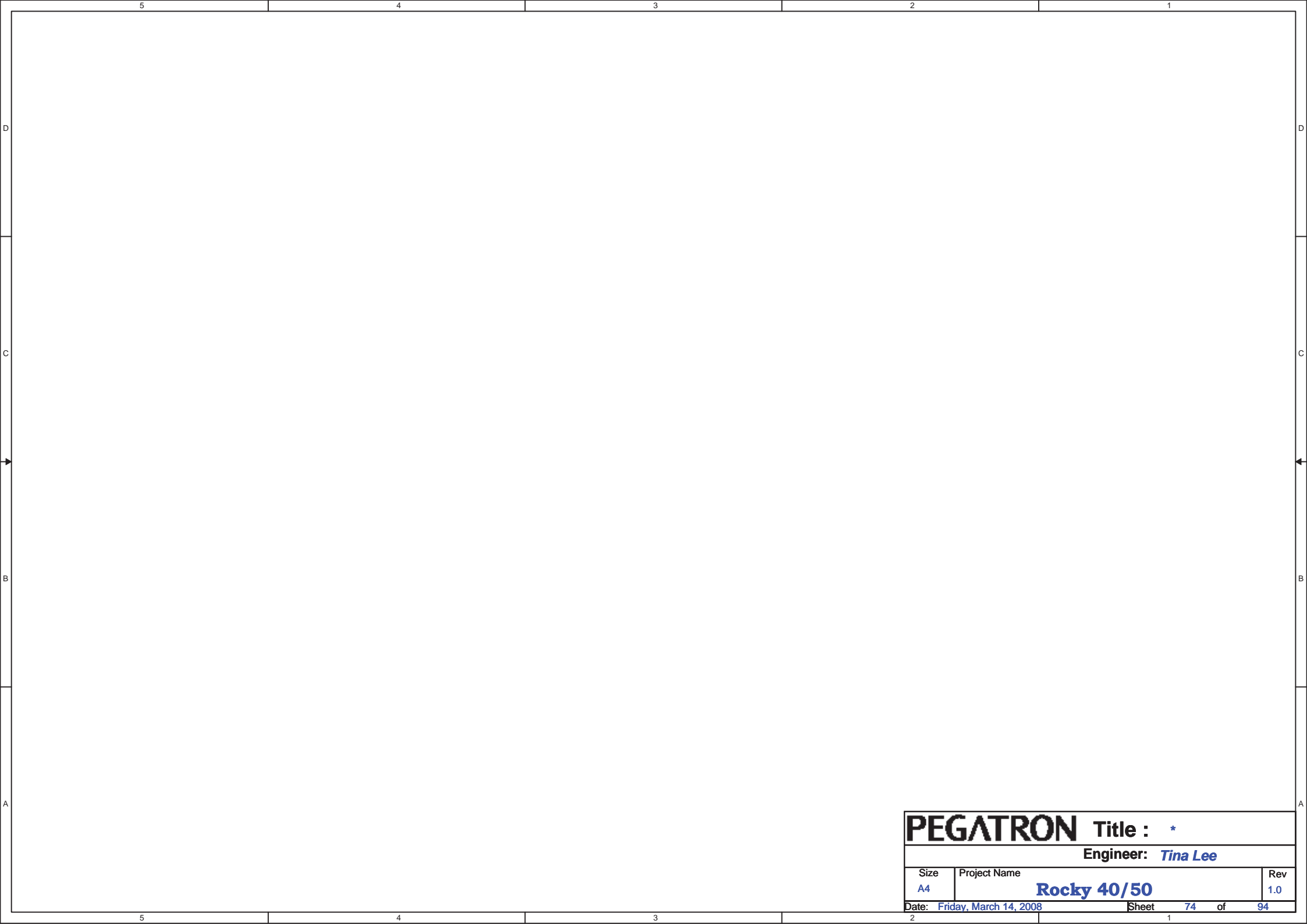
PEGATRON			Title : *	
Engineer: Tina Lee				
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	71 of 94



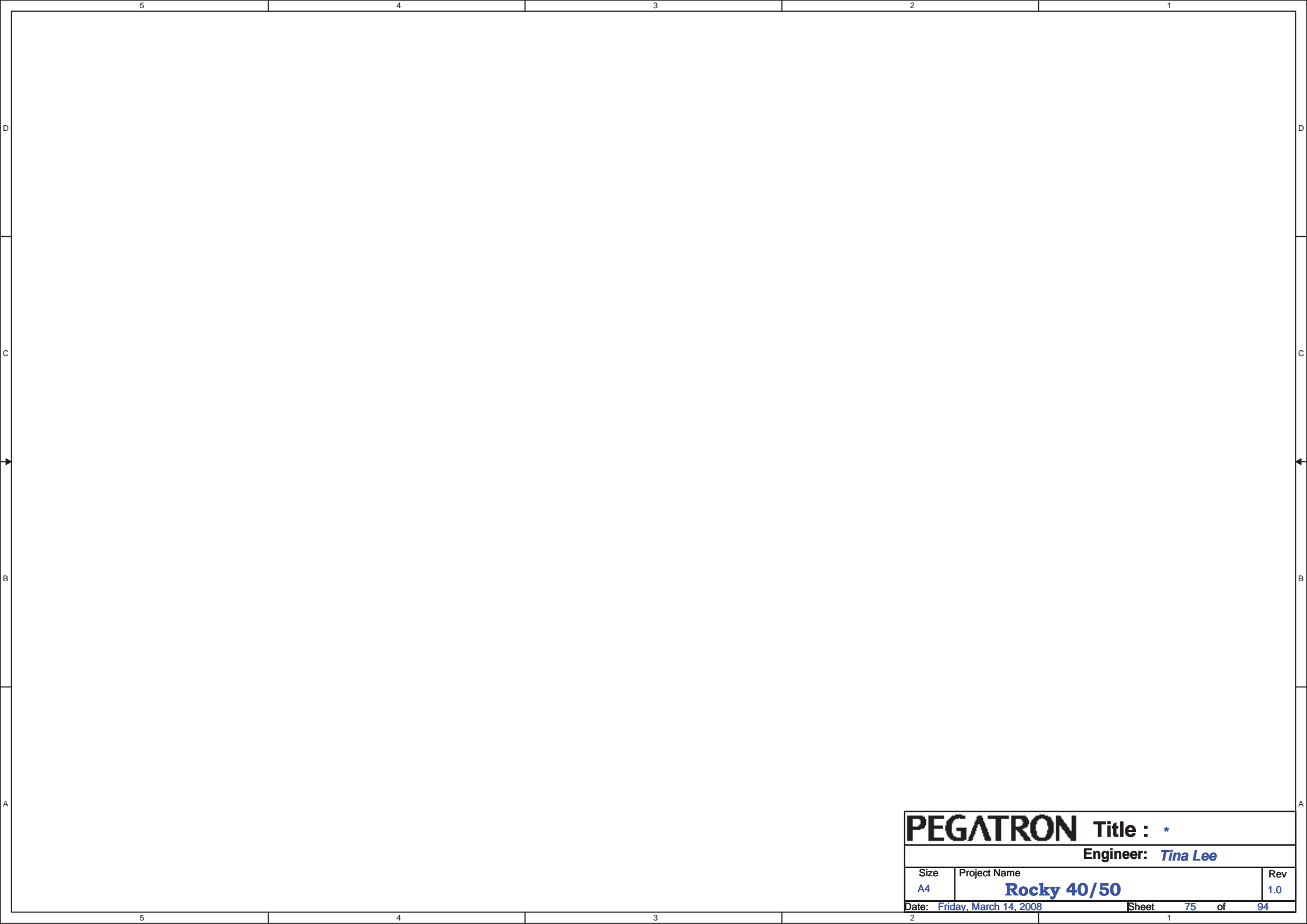
PEGATRON			Title : *	
			Engineer: Tina Lee	
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	72 of 94

5	4	3	2	1
D				D
C				C
B				B
A				A

PEGATRON			Title : *		
Engineer: Tina Lee					
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet 73 of 94		

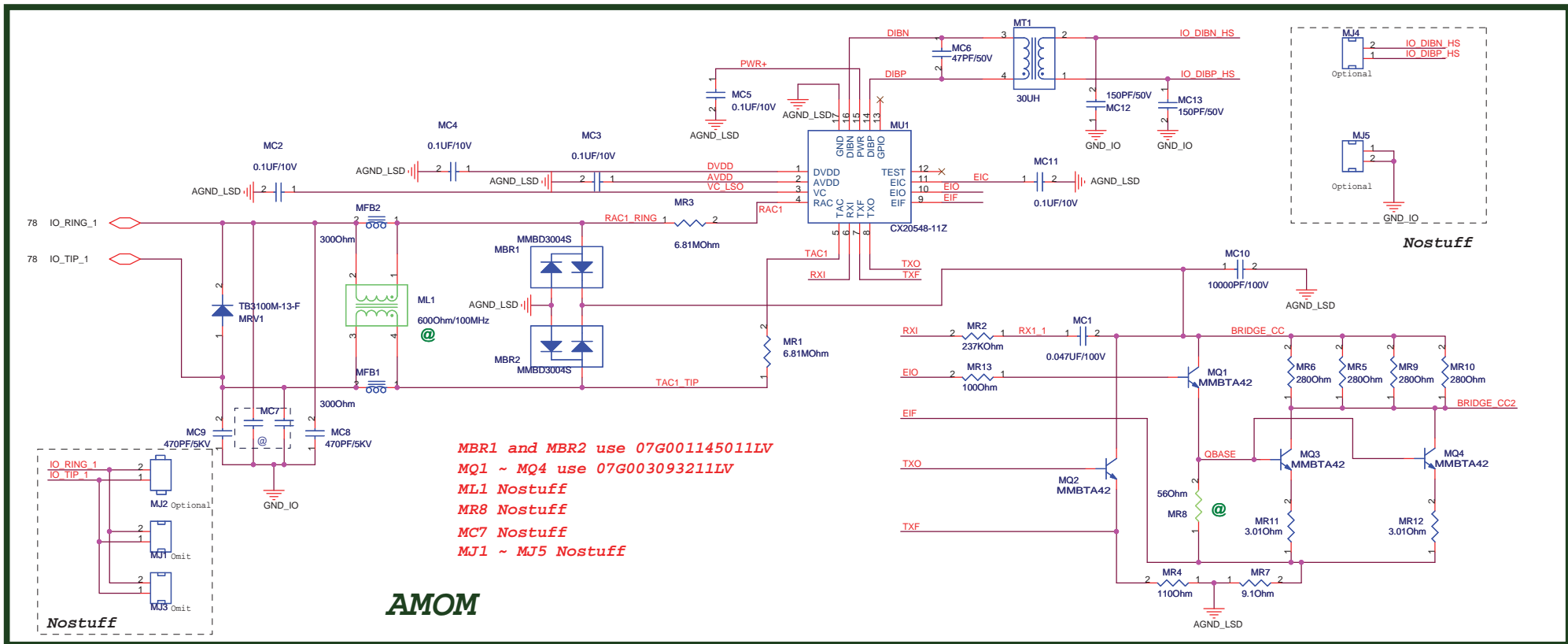
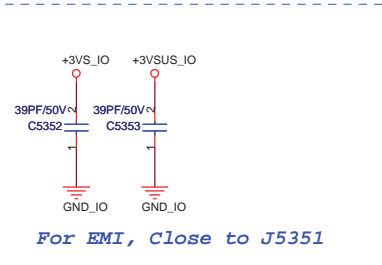
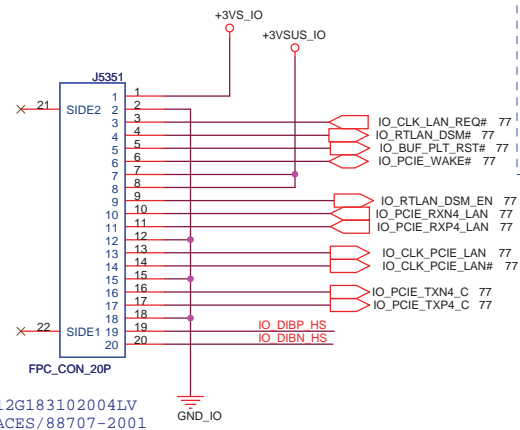


PEGATRON		Title : *	
Engineer: Tina Lee			
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	74 of 94

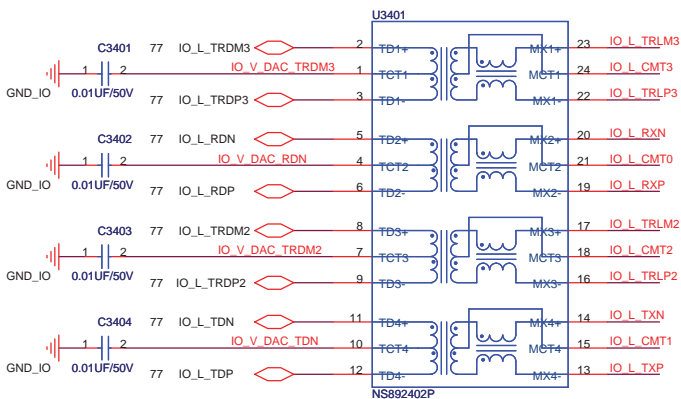
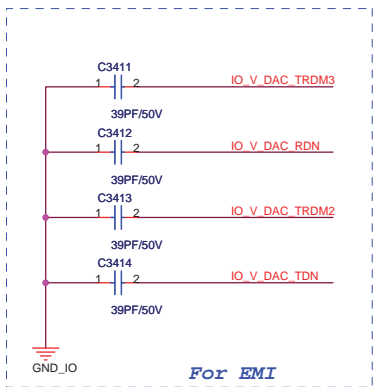


PEGATRON			Title : *		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	75	of 94

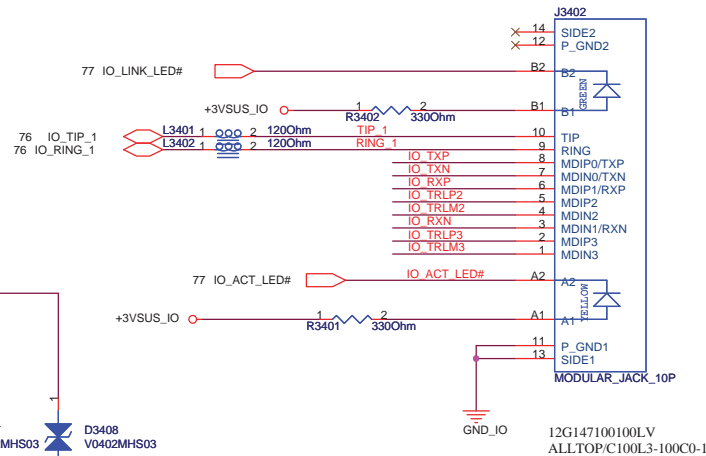
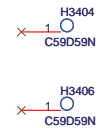
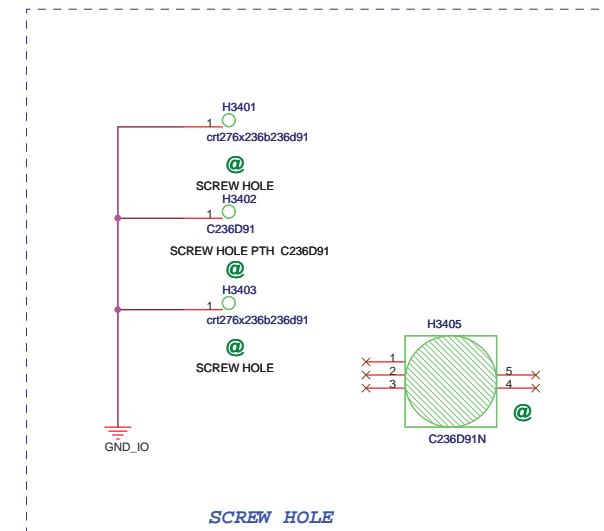
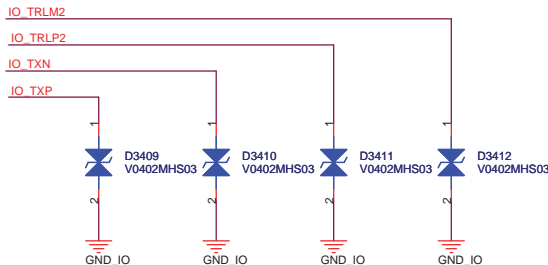
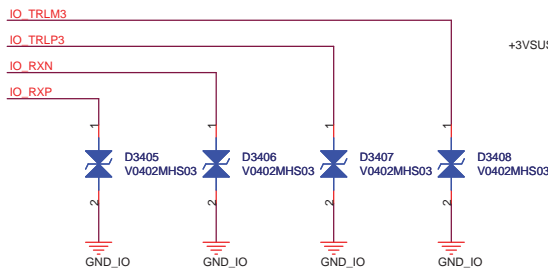
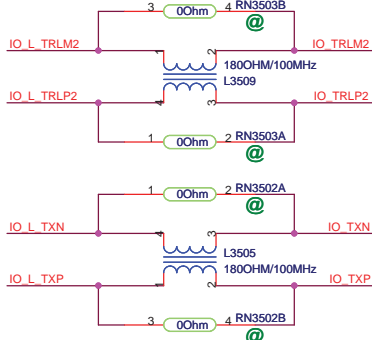
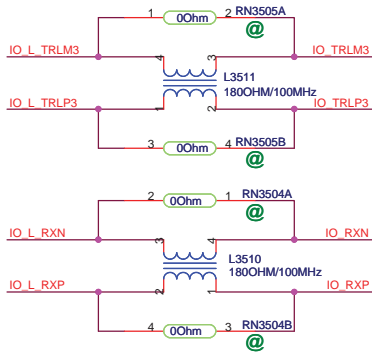
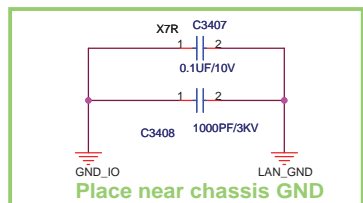
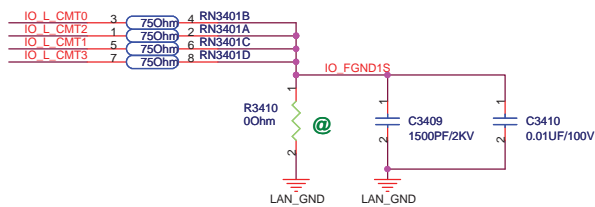
# IO BOARD



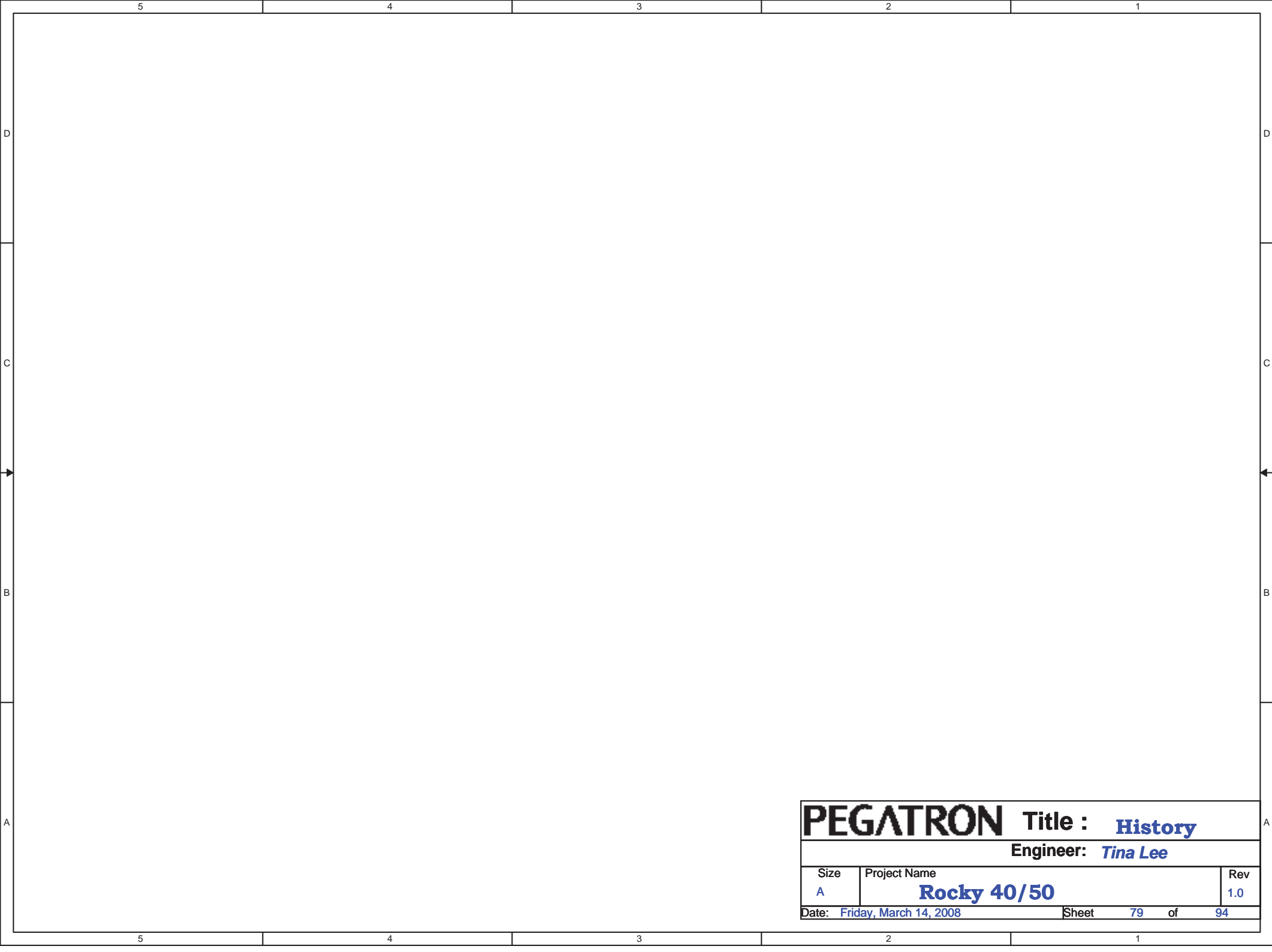




Transformer



<Variant Name>



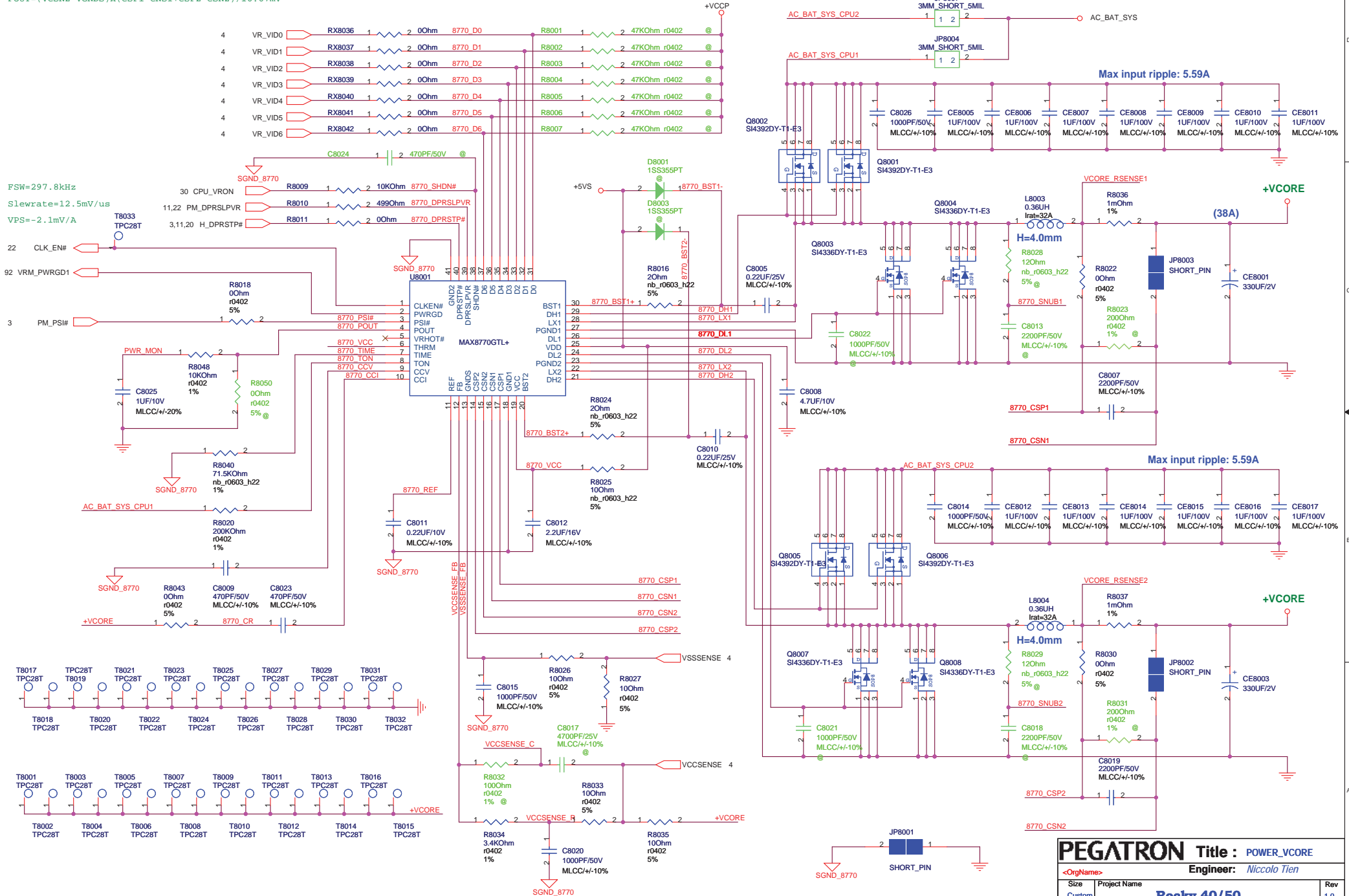
<b>PEGATRON</b>		Title : <b>History</b>	
Engineer: <b>Tina Lee</b>			
Size <b>A</b>	Project Name <b>Rocky 40/50</b>		Rev <b>1.0</b>
Date: <b>Friday, March 14, 2008</b>		Sheet <b>79</b> of <b>94</b>	

# IMVP6 CPU VCORE REGULATOR

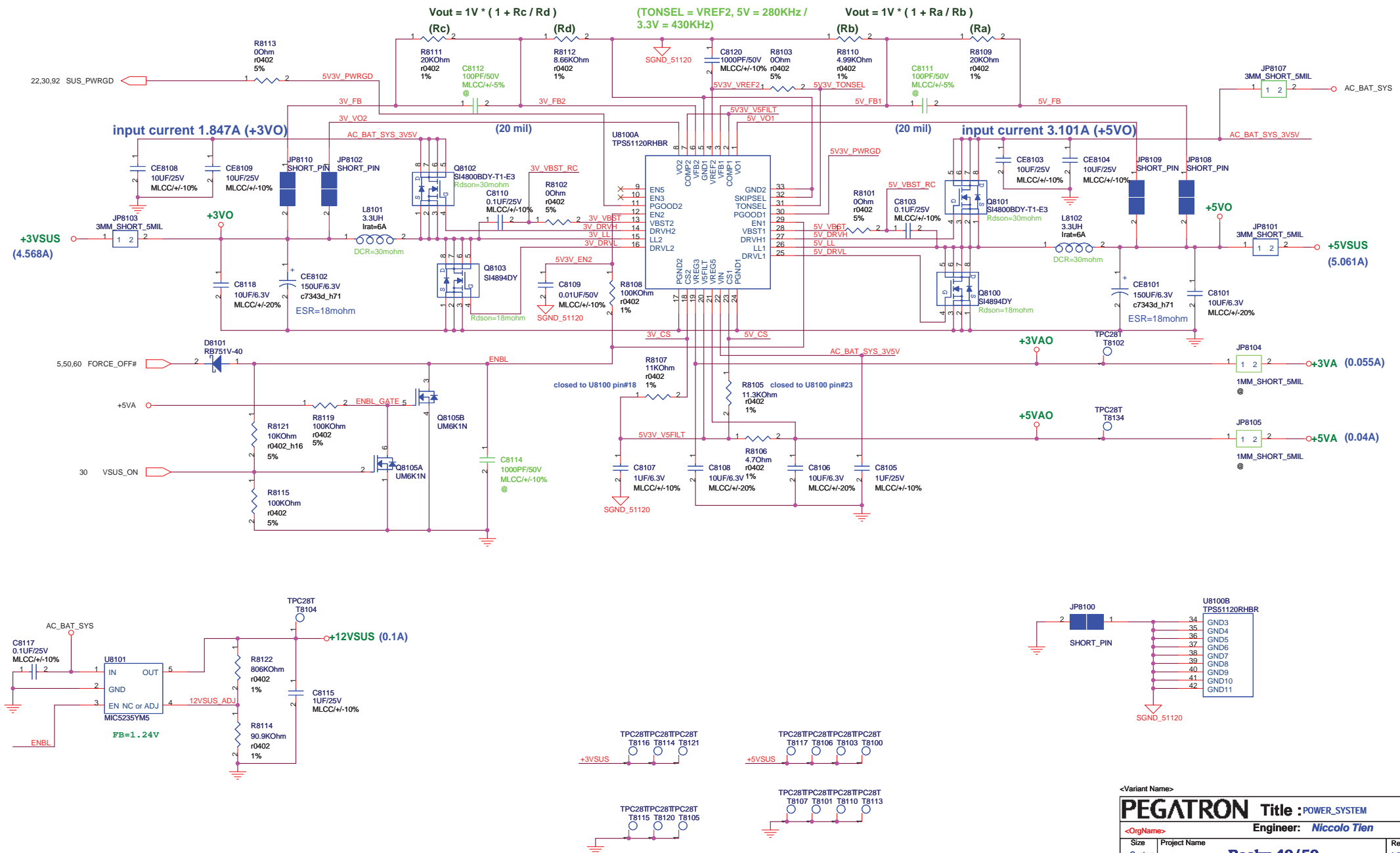
3.3V level logic level: DPRSLPVR, SHDN#

1.05V level logic: VID, PSI#, DPRSTP#

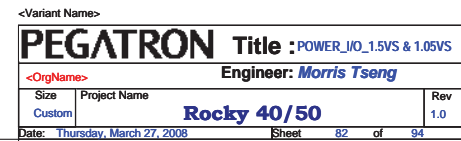
$POUT = (VCSN2 - VGND5) \times (CSP1 - CNS1 + CSP2 - CSN2) / 16.67mV$



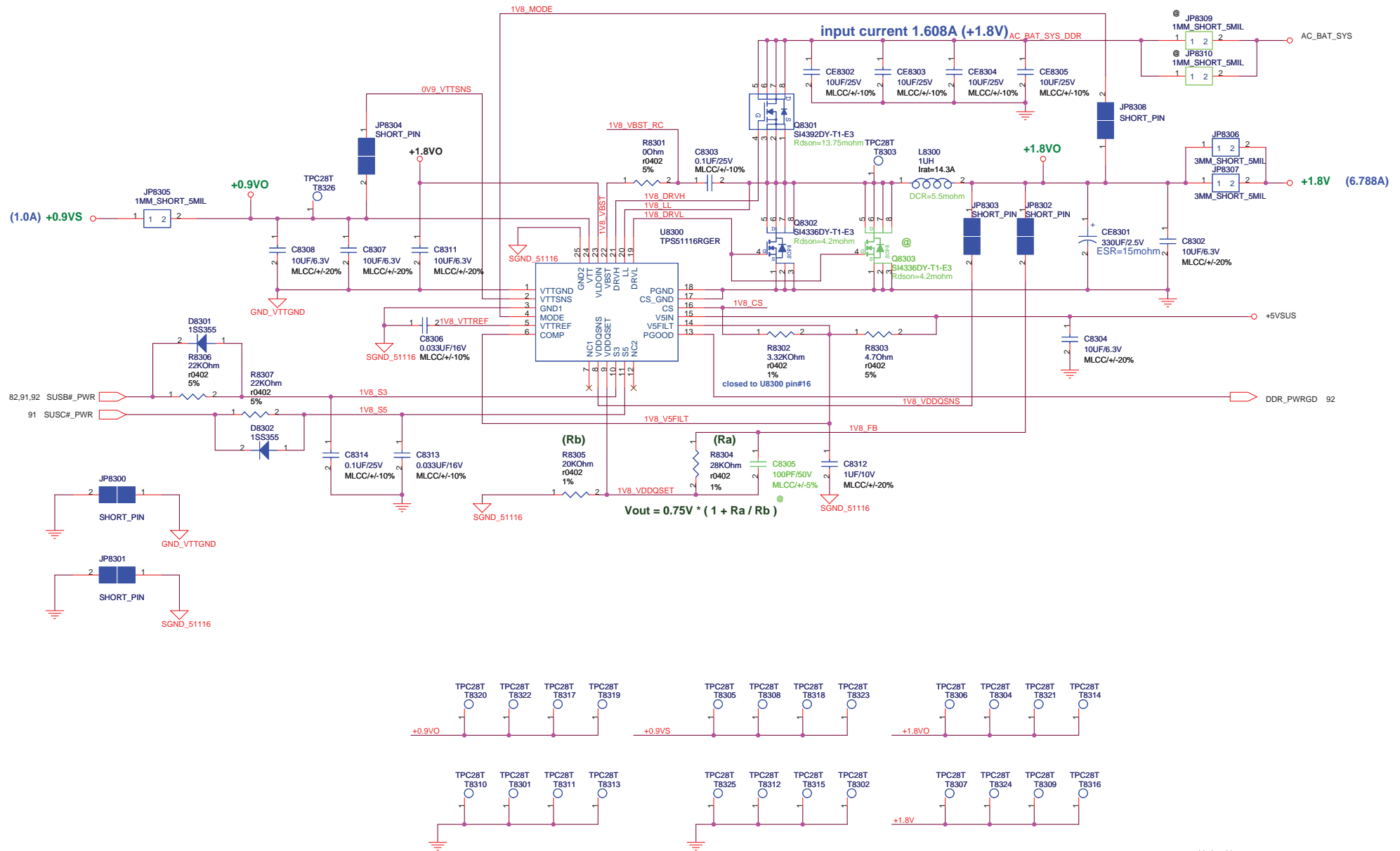
## +5V / +3.3V POWER SUPPLY



(TONSEL = FLOAT, 1.5V = 360KHz /  
1.05V = 300KHz)



## +1.8V / +0.9VS POWER SUPPLY



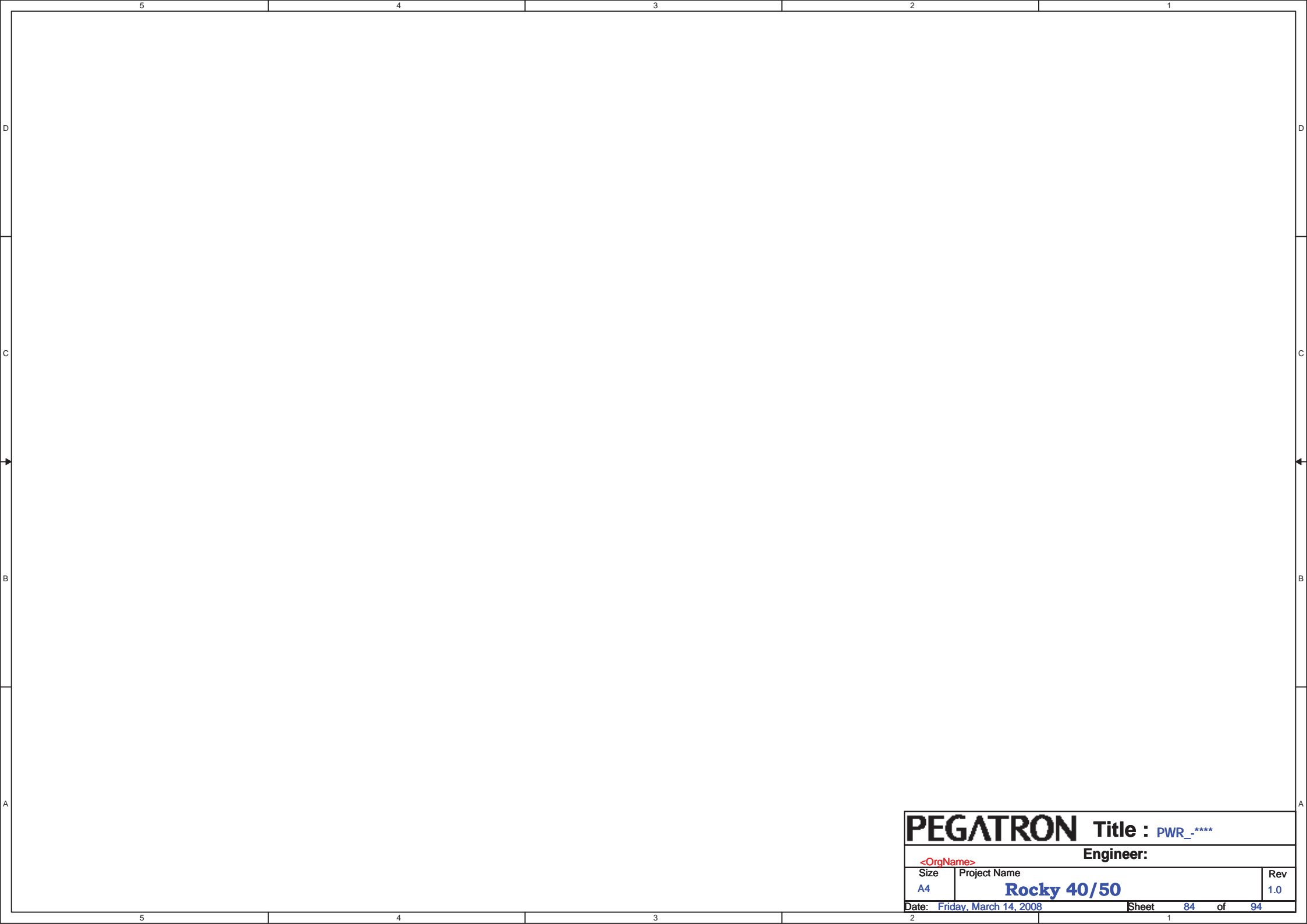
**<Variant Name>**

PEGATRON Title : POWER\_I/O\_DDR & VTT

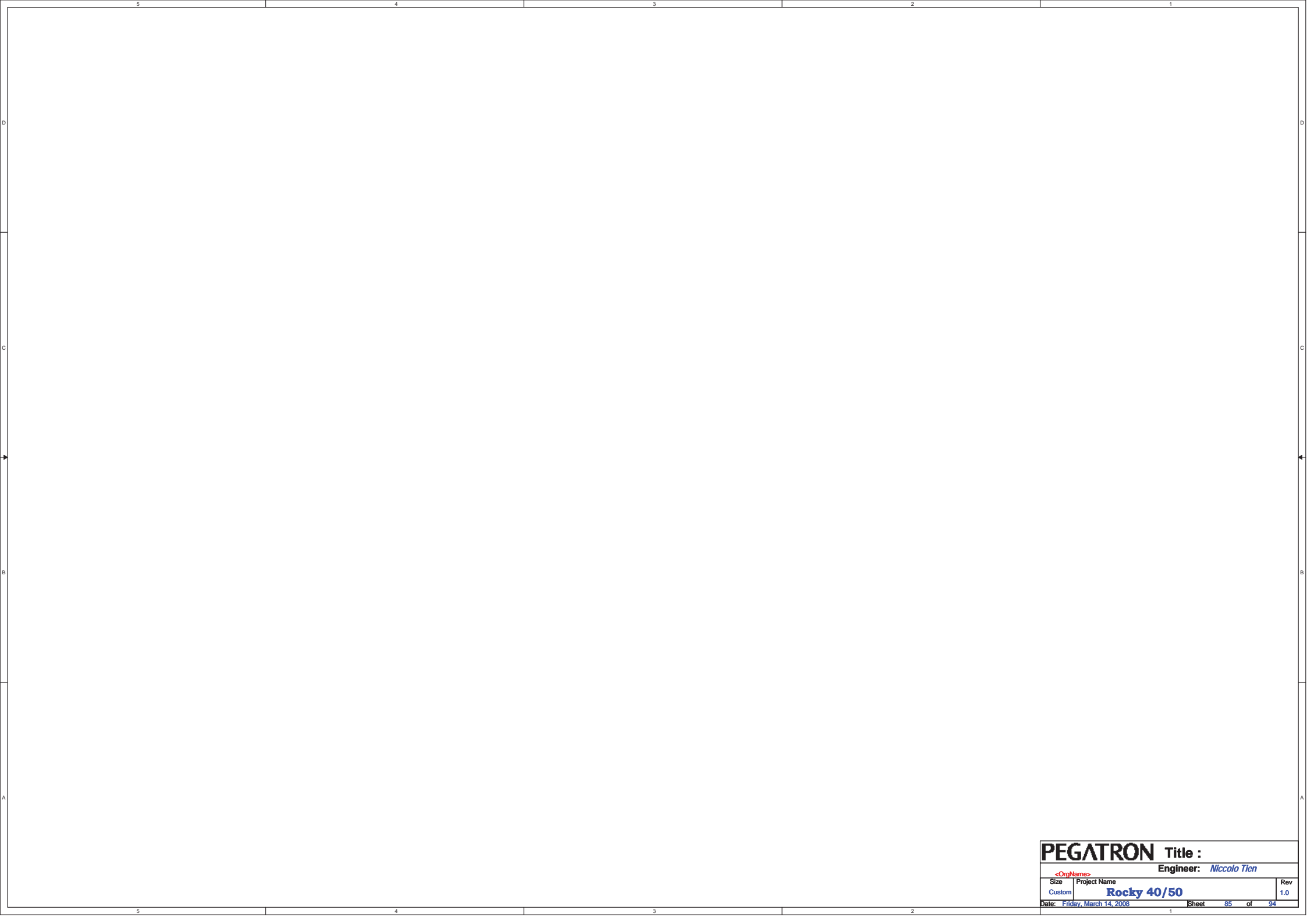
<OrgName> Engineer: **Morris Tseng**

Size	Project Name	Rev
Custom	<b>Rocky 40/50</b>	1.0

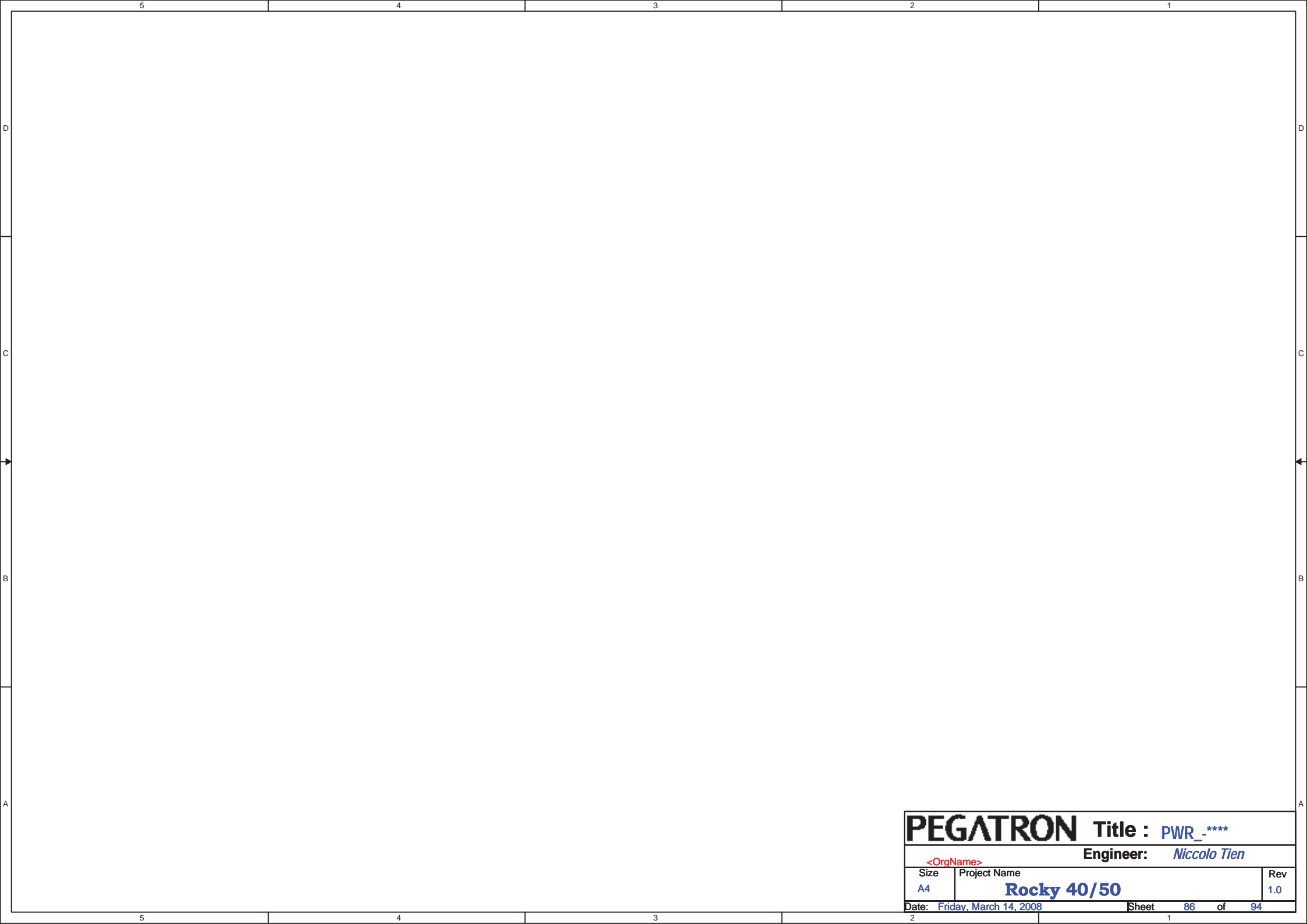
Date: Thursday, March 27, 2008 Sheet 83 of 94



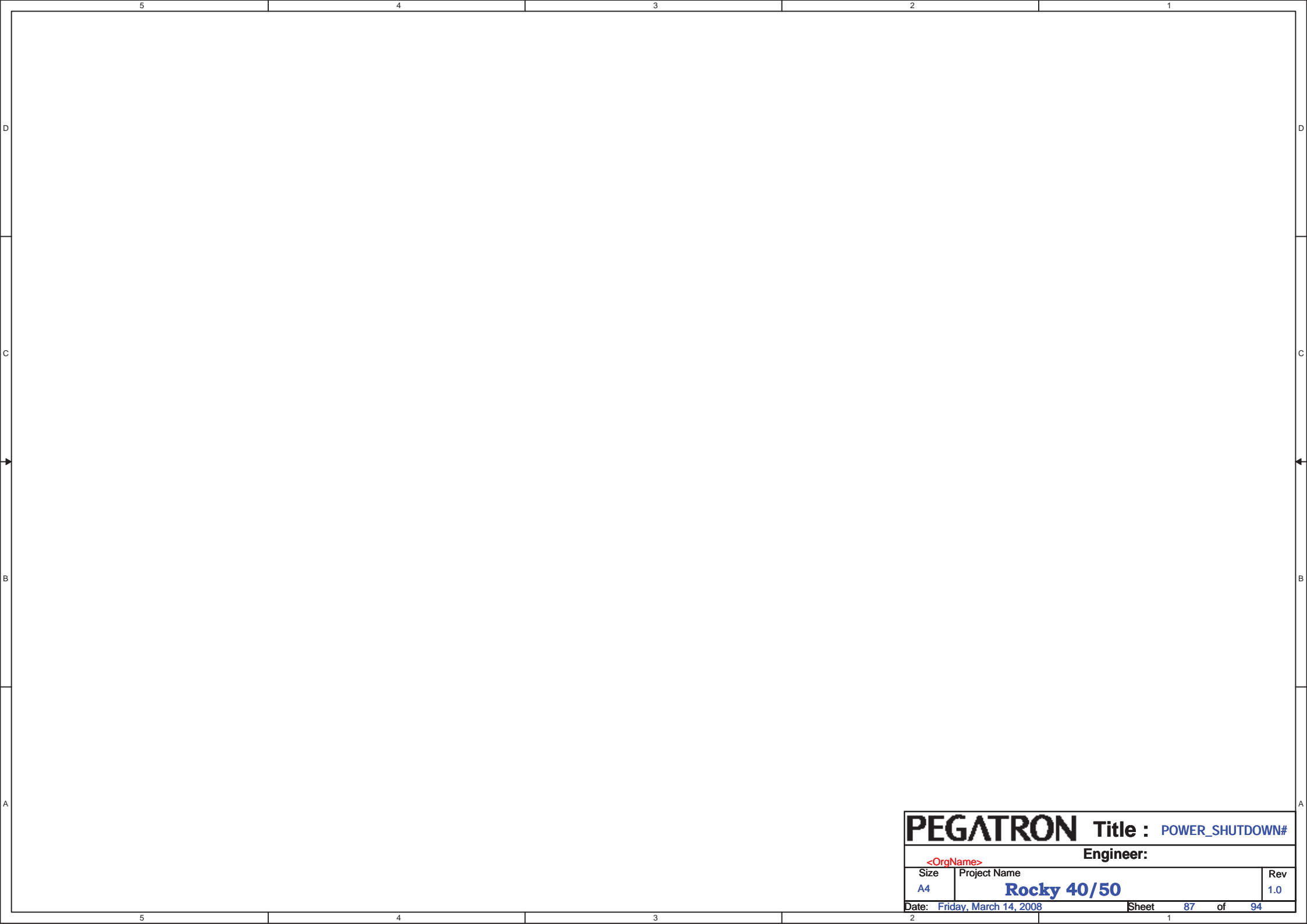
<b>PEGATRON</b>			<b>Title :</b> PWR_-****		
			<b>Engineer:</b>		
<small>&lt;OrgName&gt;</small>					
<small>Size</small>	<small>Project Name</small>				<small>Rev</small>
A4	Rocky 40/50				1.0
<small>Date:</small> Friday, March 14, 2008			<small>Sheet</small>	84	<small>of</small> 94



<b>PEGATRON</b>		<b>Title :</b>	
<OrigName>		<b>Engineer:</b> <i>Niccolo Tien</i>	
Size	Project Name		Rev
Custom	<b>Rocky 40/50</b>		1.0
Date: Friday, March 14, 2008	Sheet	85 of	94

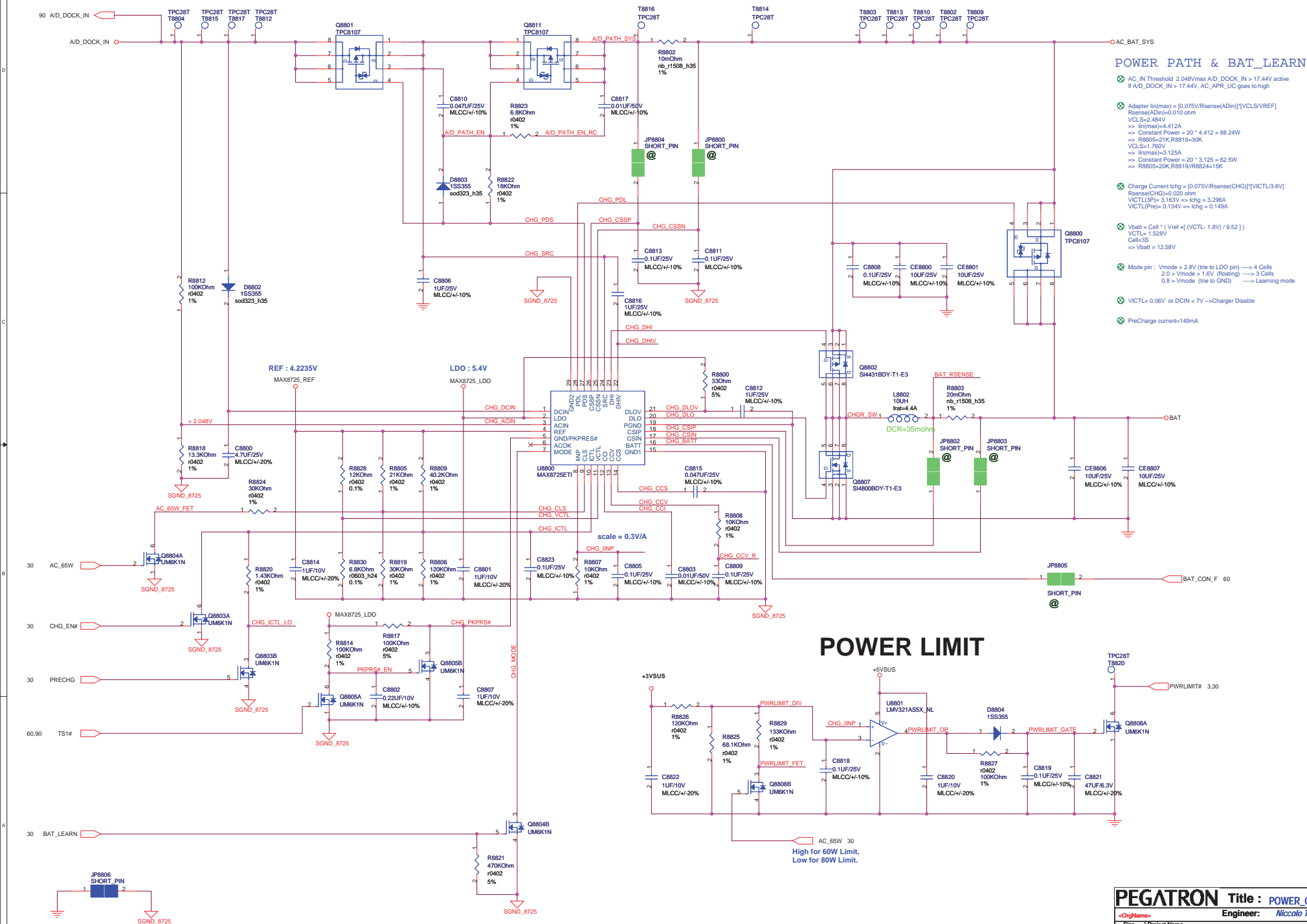


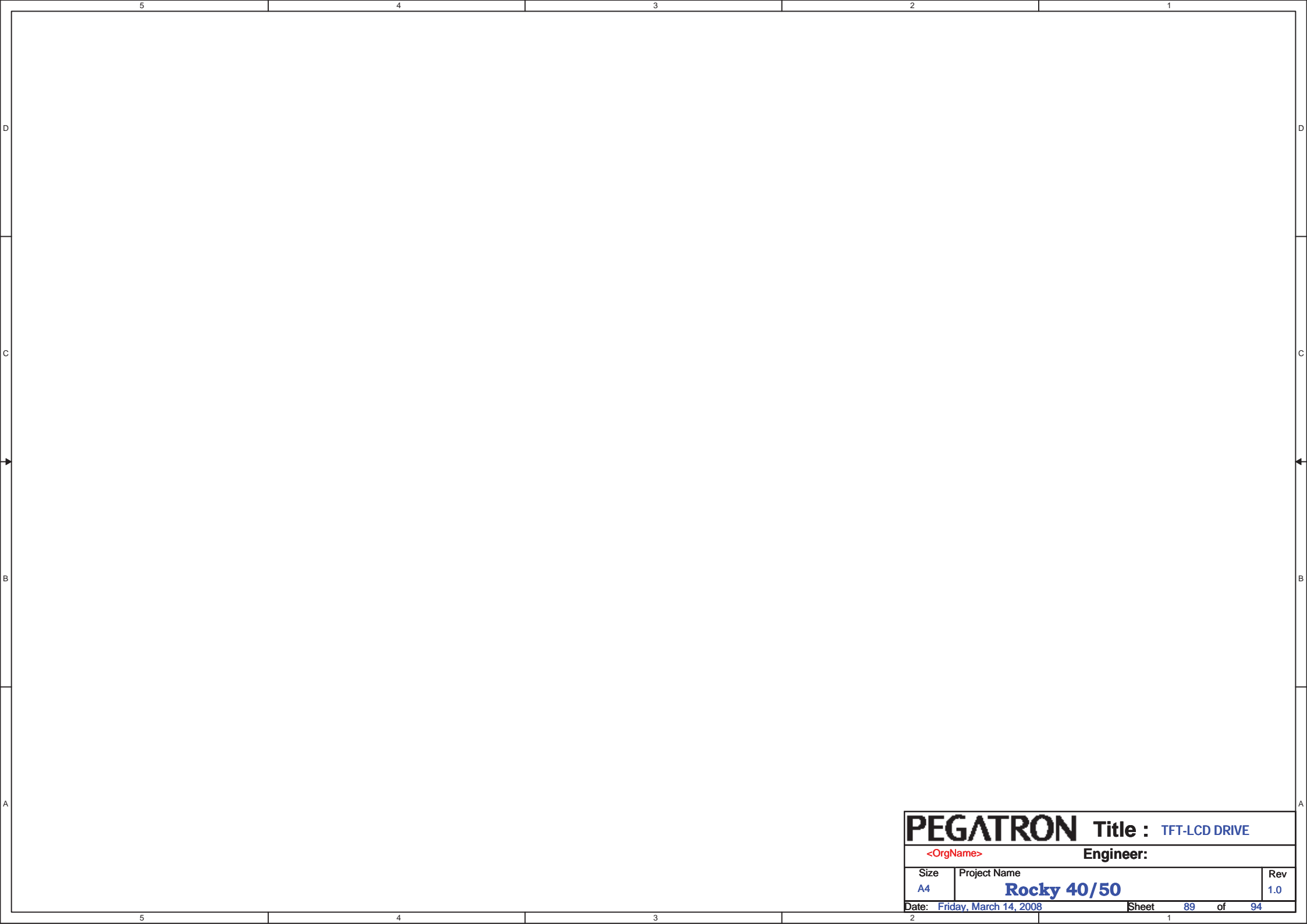
<b>PEGATRON</b>		<b>Title :</b> PWR_-****	
<OrgName>		<b>Engineer:</b> Niccolo Tien	
Size A4	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Friday, March 14, 2008		Sheet	86 of 94



<b>PEGATRON</b>		<b>Title :</b> POWER_SHUTDOWN#	
<b>Engineer:</b>			
<OrgName>			
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	87 of 94

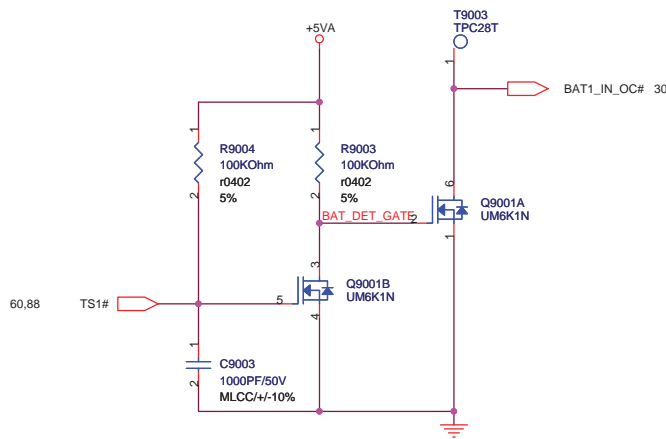
# BATTERY CHARGER



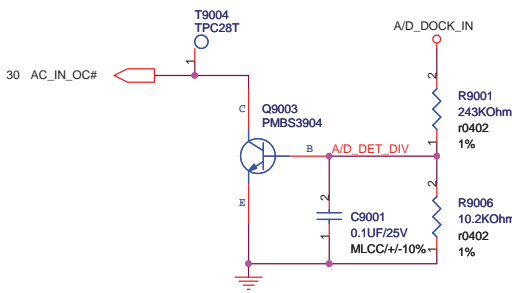


PEGATRON		Title : TFT-LCD DRIVE	
<OrgName>		Engineer:	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	89 of 94

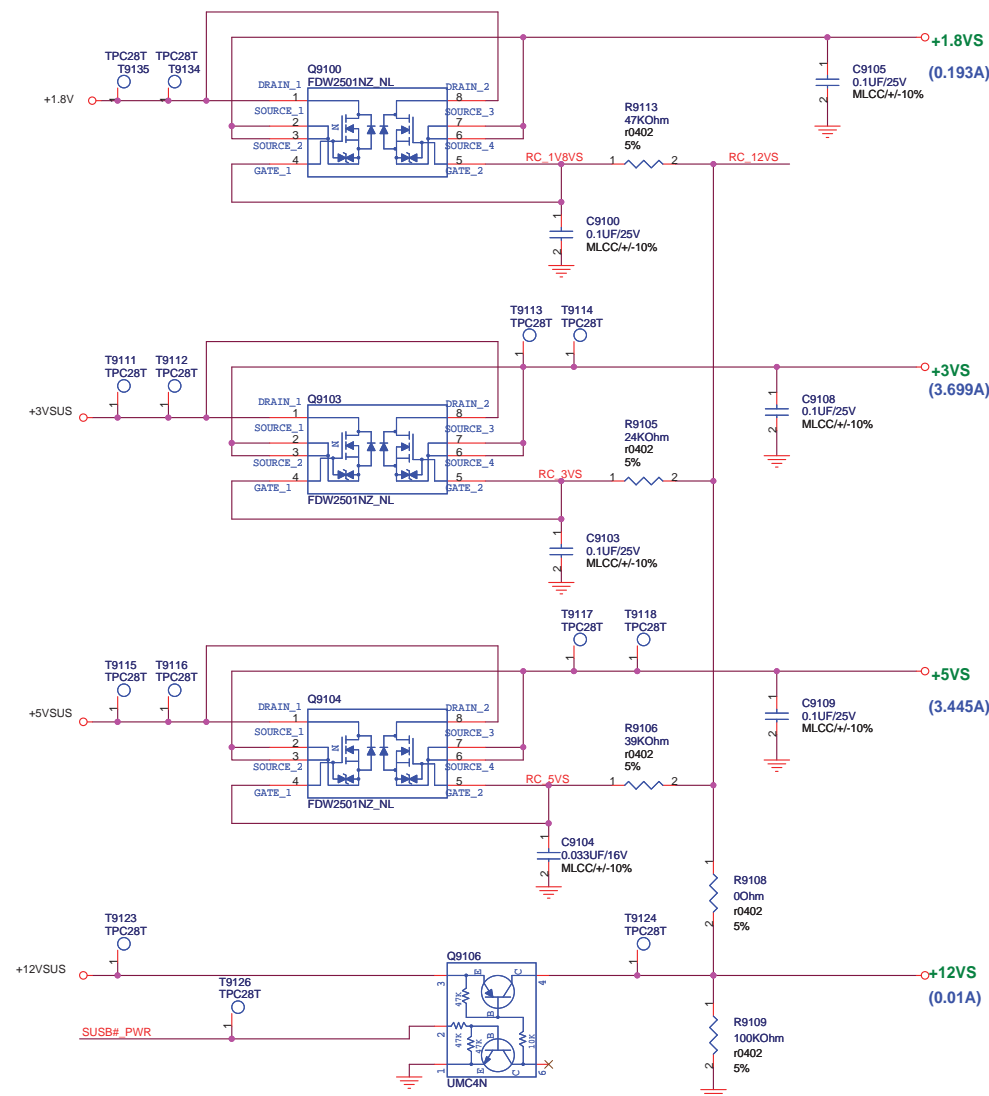
BATTERY IN DETECT



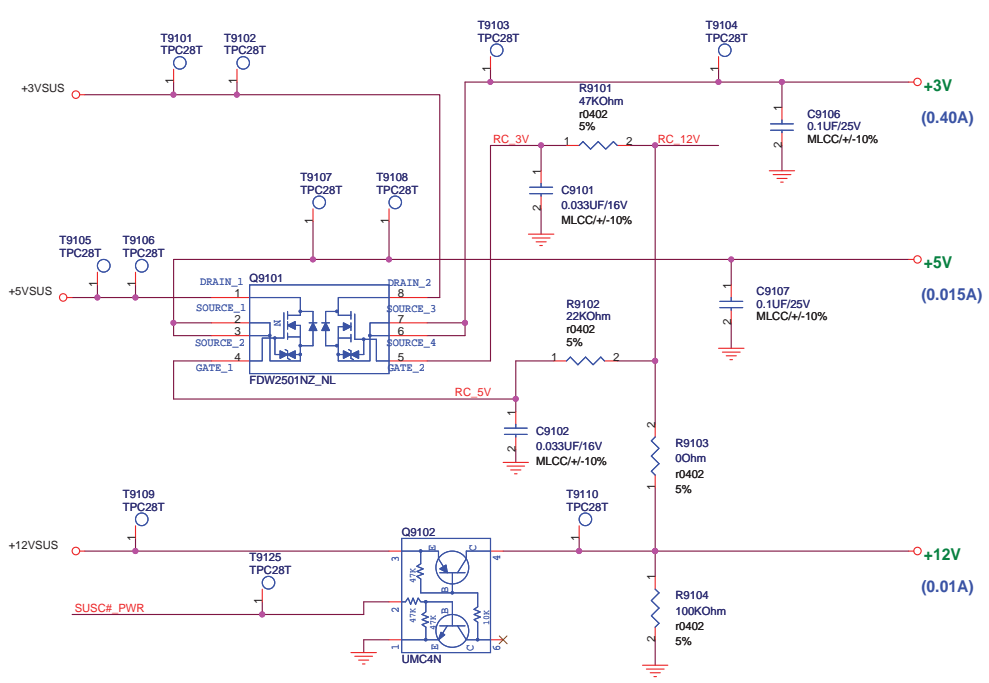
ADAPTER IN DETECT



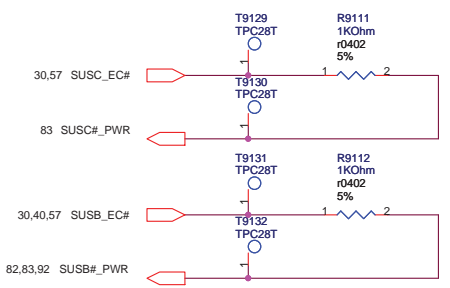
SUSB#\_PWR Load SW



SUSC#\_PWR Load SW



Enable Signal



<b>PEGATRON</b>		<b>Title :</b> POWER_PROTECT	
<b>Engineer:</b> Niccolo Tien			
<b>Size</b> Custom	<b>Project Name</b> <b>Rocky 40/50</b>	<b>Rev</b> 1.0	
<b>Date:</b> Thursday, March 27, 2008	<b>Sheet</b> 92	<b>of</b> 94	

