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III Semester BE-CSE

Subject Name: CS2202 Digital Principles and System Design

Important 16 Marks Questions Unit I –V

1. Simplify the following Boolean expression using Quine McCluskey method:
 $F = \sum m(0, 9, 15, 24, 29, 30) + d(8, 11, 31)$
2. Simplify the expression $F(A, B, C, D) = (1, 4, 6, 7, 8, 9, 10, 11, 15)$ using Quine-McClusky method
3. Explain the conversion of regular expression in to canonical expression and their simplification in SOP and PS form
4. Reduce the Boolean function using K Map technique and implement using gates $F(w, x, y, z) = \sum (0, 1, 4, 8, 9, 10)$ which has the don't care conditions $d(w, x, y, z) = \sum (2, 11)$.
5. State and prove DeMorgan's Theorem
6. Simplify the function using tabulation method, $F(w, x, y, z) = \sum (1, 2, 3, 5, 9, 12, 14, 15) + d(4, 8, 11)$
7. Design a combinational circuit to convert BCD to Excess code and Design a Excess-3 to BCD converter.
8. Explain BCD adder with a neat block diagram and Design a combinational circuit to convert binary to gray code
9. Design a 4 bit magnitude comparator
10. Explain the gray code to binary converter with the necessary diagram
11. With neat diagram explain BCD subtractor using 9's and 10's complement method
12. Explain with necessary diagram a BCD to 7 segment display decoder
13. Design a parity checker
14. Design a 4-bit priority encoder
15. Design a BCD to excess-3 code converter and implement using PLA
16. Implement switching function $F = \sum (0, 1, 3, 4, 12, 14, 15)$ using a 4 and 8 input MUX
17. Define Decoder. Design a 3 to 8 decoder. With suitable block diagram explain how a 4 to 16 decoder can be performed by using the same.
18. Explain the different types of shift registers with neat diagram.
19. Design a sequential circuit with JK flip Flop
20. Using D flip-flops, design a synchronous counter which counts in the sequence, 000, 001, 010, 011, 100, 101, 110, 111, 000
21. Design and implement a Mod-5 synchronous counter using JK flip-flop
22. With a neat circuit explain a universal shift register
23. Design a Mod 6 counter using SR flip flops and explain a 4 bit ripple counter
24. Write details on hazards in combinational circuit and sequential circuits
25. Explain the steps for the design of asynchronous sequential circuits
26. Develop the state diagram and primitive flow table for a logic system that has 2 inputs, x and y and an output z. And reduce primitive flow table. The behaviour of the circuit is stated as follows.
Initially $x = y = 0$. Whenever $x = 1$ and $y = 0$ then $z = 1$, whenever $x = 0$ and $y = 1$ then $z = 0$. When $x = 0$ or $x = y = 1$ no change in z it remains in the previous state. The logic system has edge-triggered inputs without having a clock. The logic system changes state on the rising edges of the 2 inputs. Static input values are not to have any effect in changing the z output